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MS-7393

Version: 0B

CPU: Intel Pentium 4 Cedar Mill / Prescott , Pentium D Smithfield / Presler and Conroe / Kentsfield family processors in LGA775 Package.

System Chipset:

NVIDIA MCP73

On Board Device:

BIOS -- SPI Flash 4M
Azalia Codec -- ALC888
LPC Super I/O -- FINTEK F71882FG
LAN -- Realtek RTL8211BL-GR
CLOCK Gen -- Integrated in MCP73

Main Memory:

Dual-channel DDR-II * 2 (Max 4GB)

Expansion Slots:

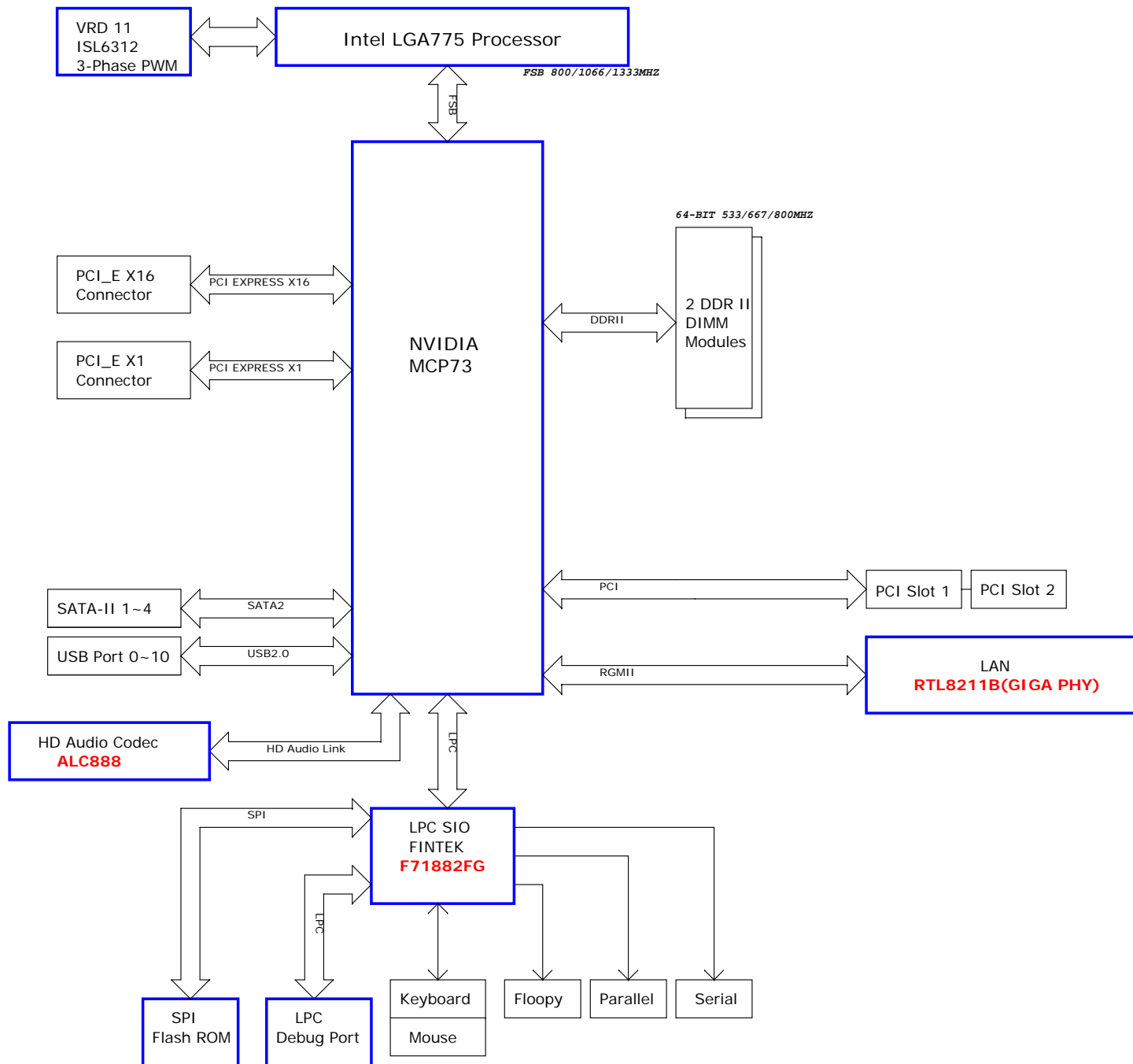
PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 2

Intersil PWM:

Controller: Intersil ISL6312 (3 Phases)

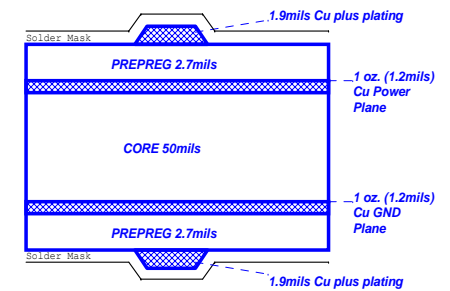
PCB = 245mm X 220mm 4L

Block Diagram



Board Stack-up

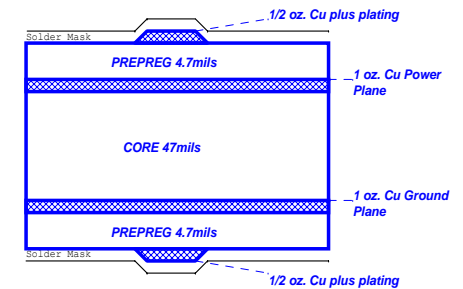
(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15
 IEEE1394 - 110ohm : 15/4/9/4/15
 IDE : 15/4/8/4/15

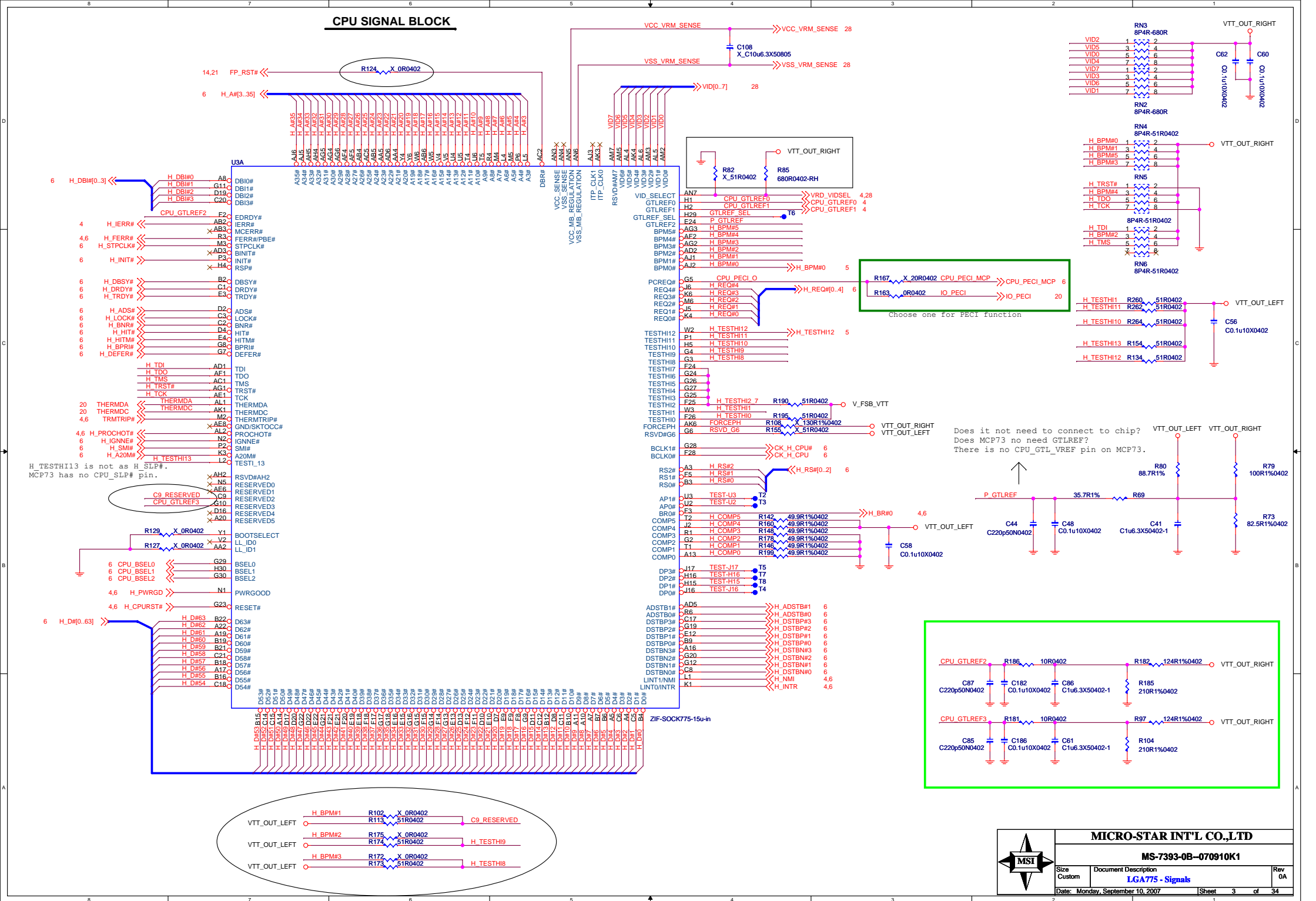
Board Stack-up

(2116 Prepreg Considerations)

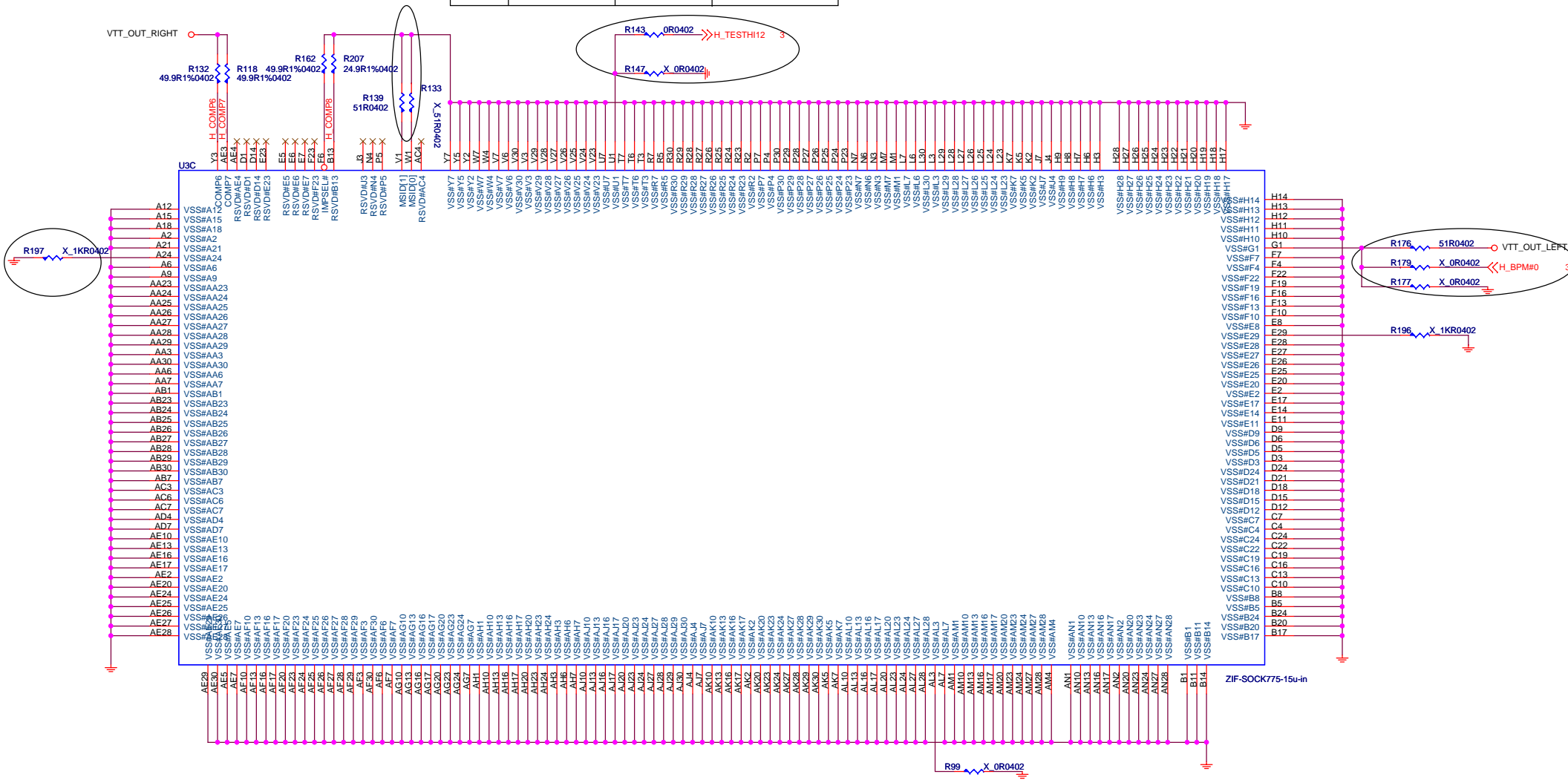


Single End 60ohm Top/Bottom : 5mils
 IEEE1394 - 110ohm Top : 5/7/5
 PCIE, LAN, SATA - 100ohm Top : 5/6/5
 USB2.0 - 90ohm Top : 7.5/7.5/7.5

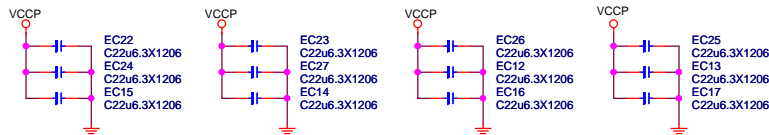
CPU SIGNAL BLOCK




	05B (130W)	05A (95W)	2006 65W FSB
MSID1	pull-down	pull-down	NC
MSID0	pull-down	NC	NC



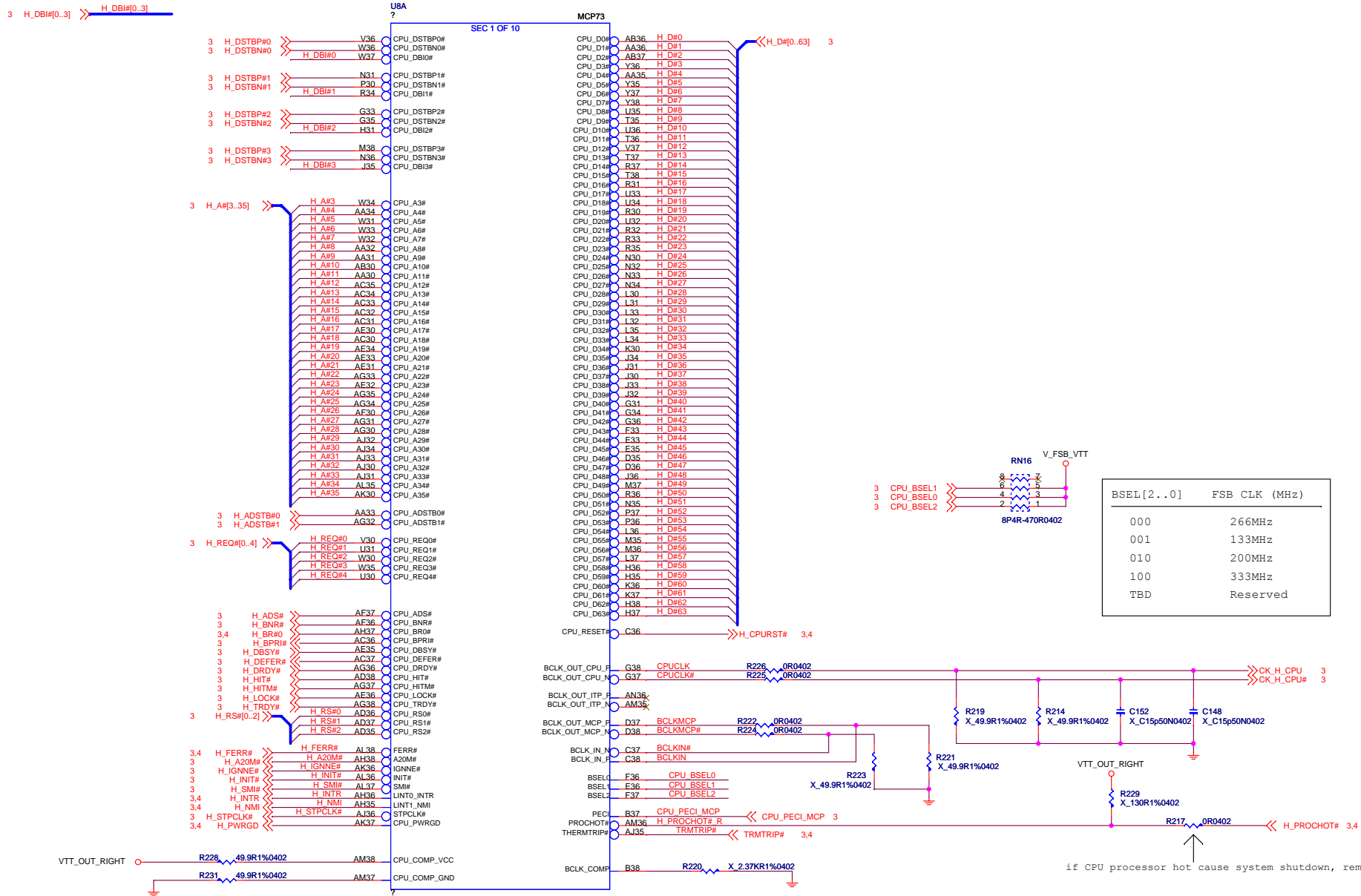
CPU DECOUPLING CAPACITORS



Place these caps within socket cavity



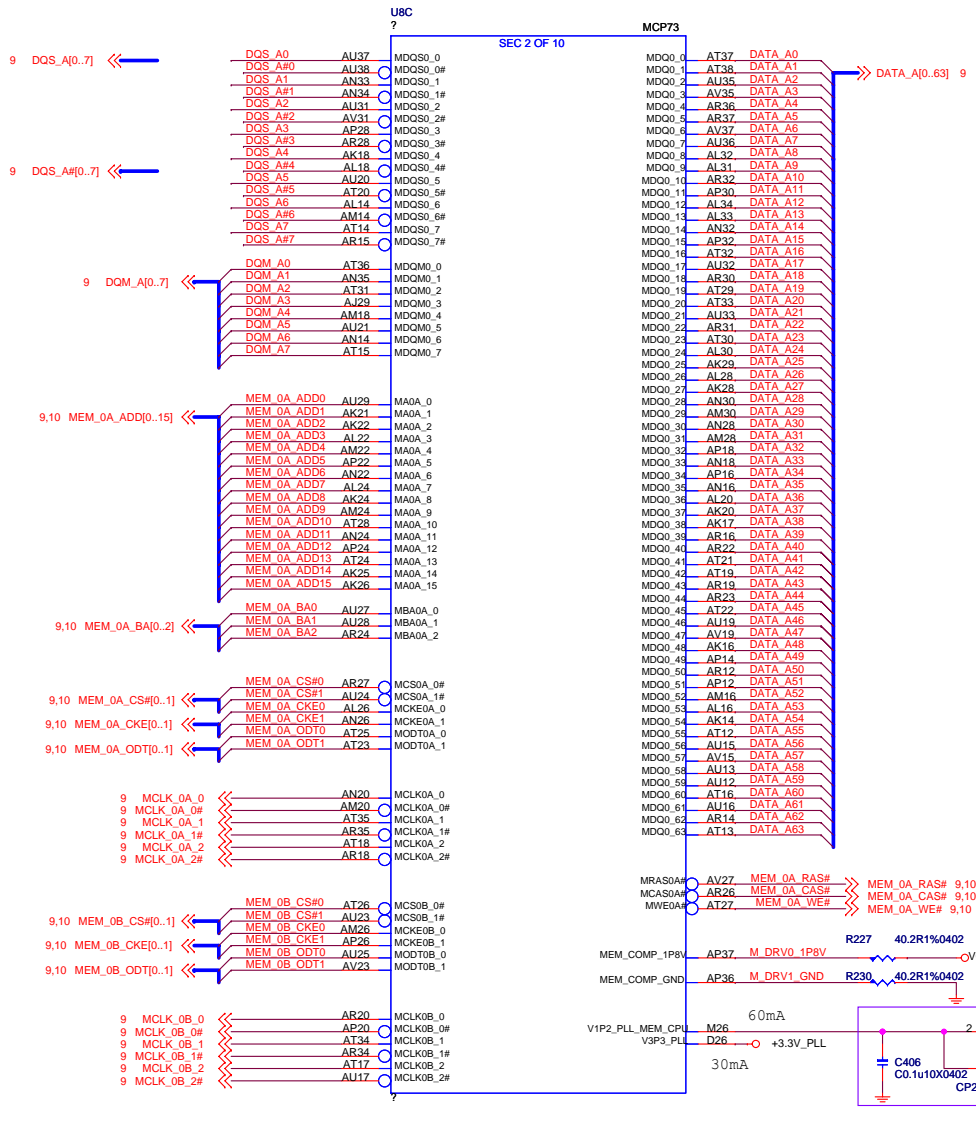
MICRO-STAR INT'L CO.,LTD		
MS-7393-0B-070910K1		
Size Custom	Document Description LGA775 - GND	Rev 0A
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DATA 0

	DIMM 1	ADDR 0A / CNTL 0A
	DIMM 2	ADDR 0B / CNTL 0B

DIMM 0A

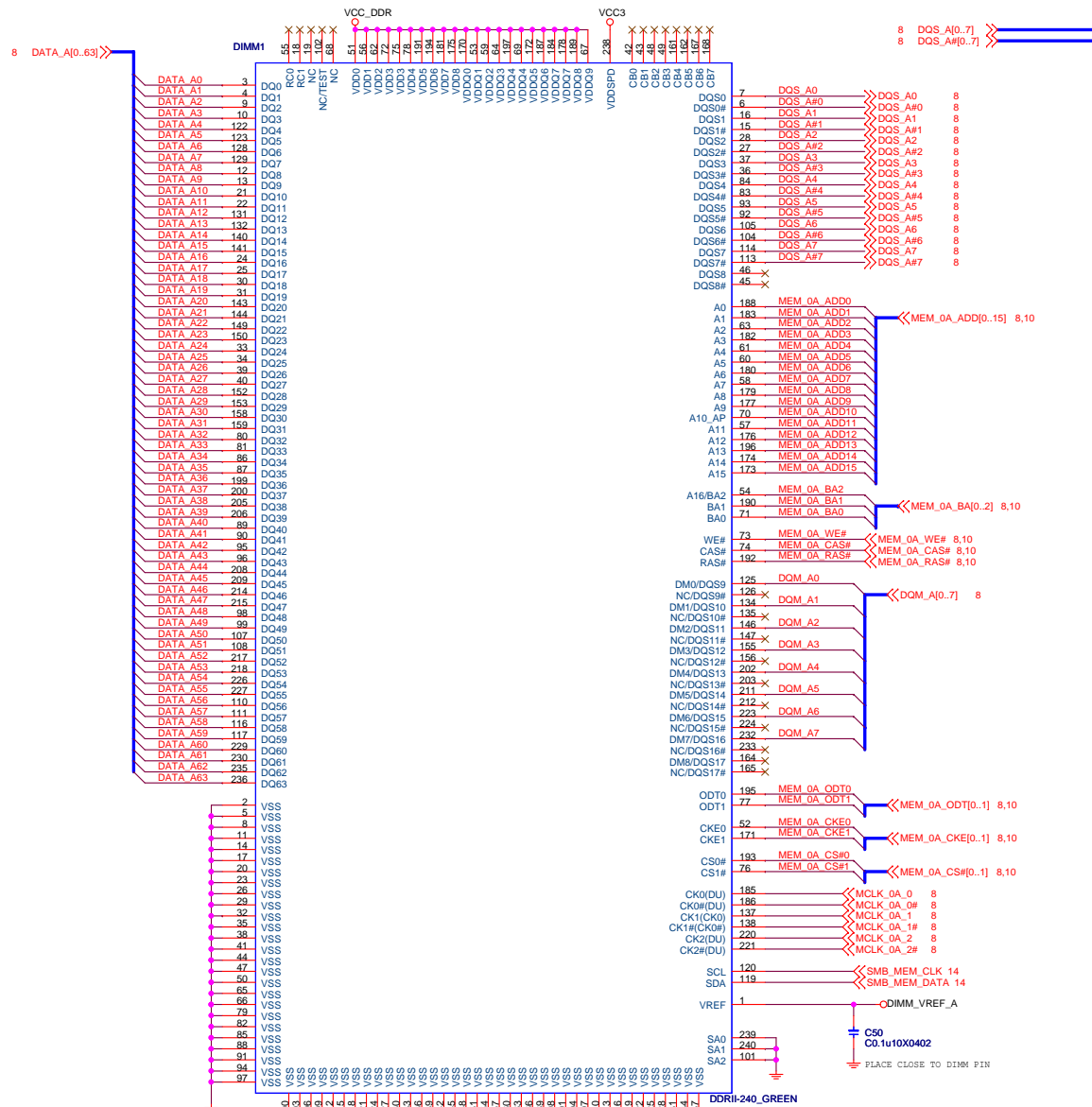


MICRO-STAR INT'L CO.,LTD

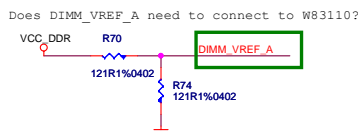
MS-7393-0B-070910K1

Size	Document Description	Rev
Custom	MCP73-MEM	0A
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DIMM1 / 0A



**ADDRESS: 000
0xA0**



**ADDRESS: 001
0xA2**

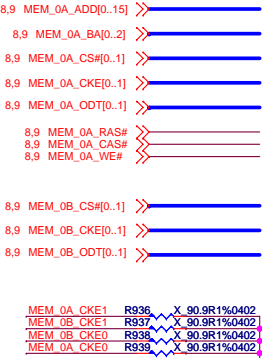
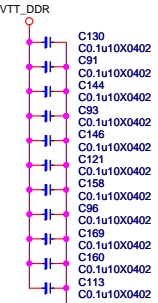
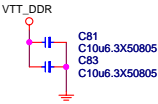


MICRO-STAR INT'L CO.,LTD

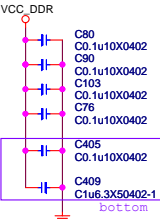
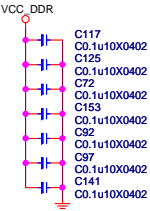
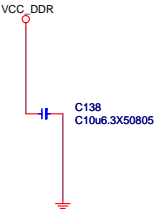
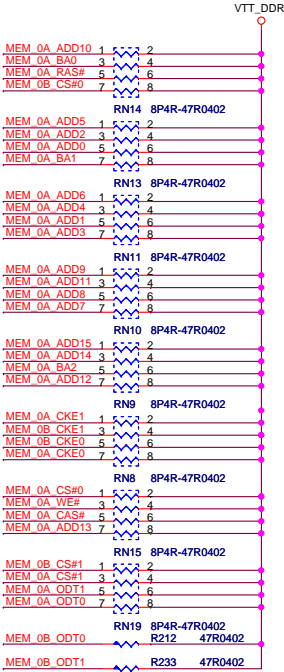
MS-7393-0B--070910K1

Size Custom	Document Description DDR II - DIMM 1 & 2 Sockets	Rev 0A
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CHANNEL A VTT_DDR DECOUPLING CAPS

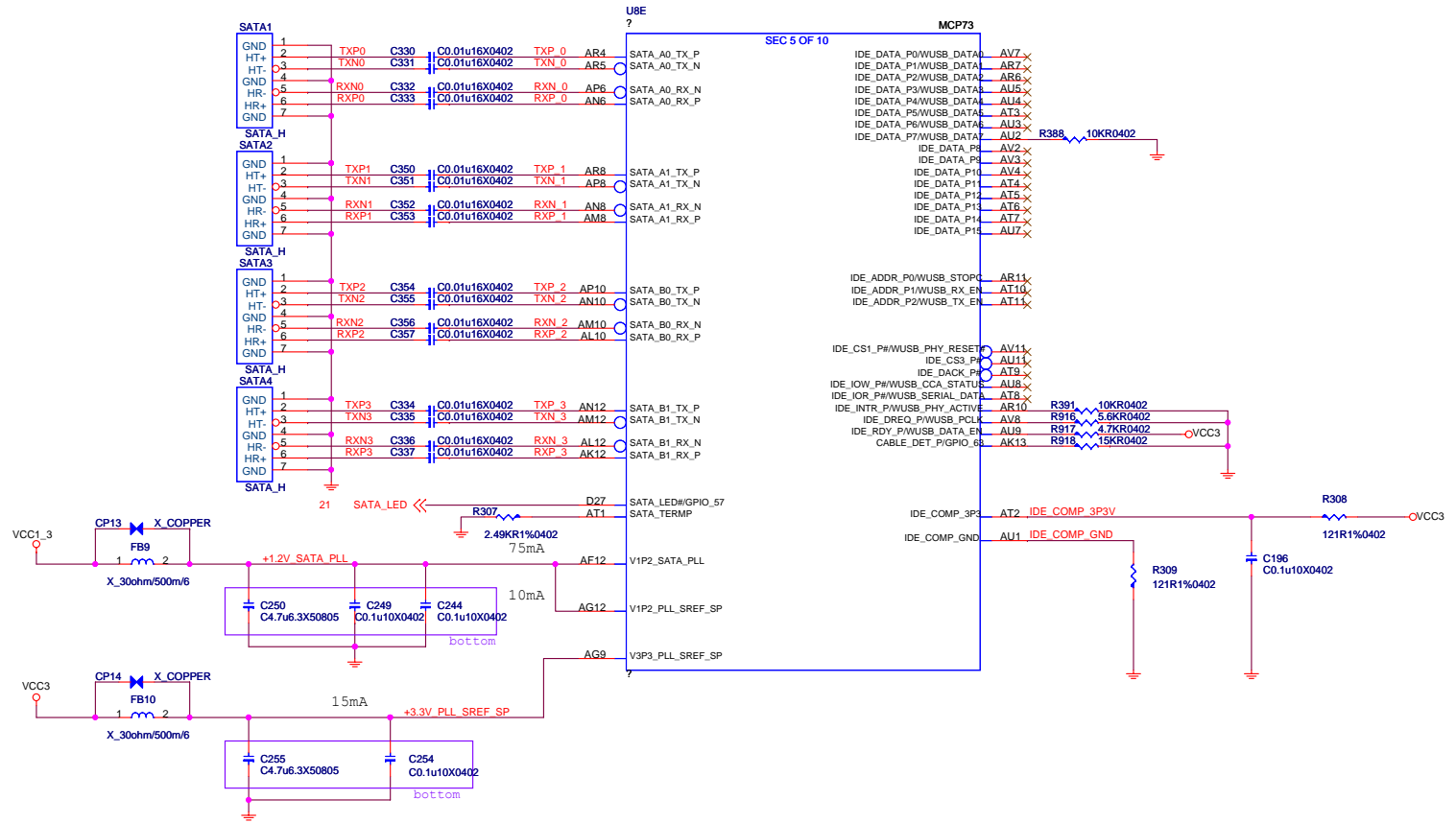


CHANNEL A ----- 0A , 0B



公板上0.1u X5, 1uX3, 10uX3
兩根再x2

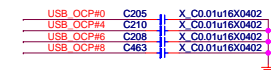
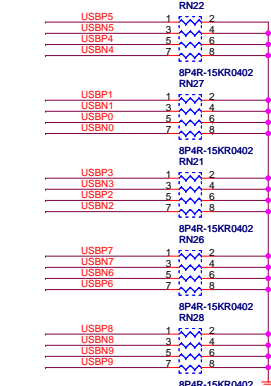
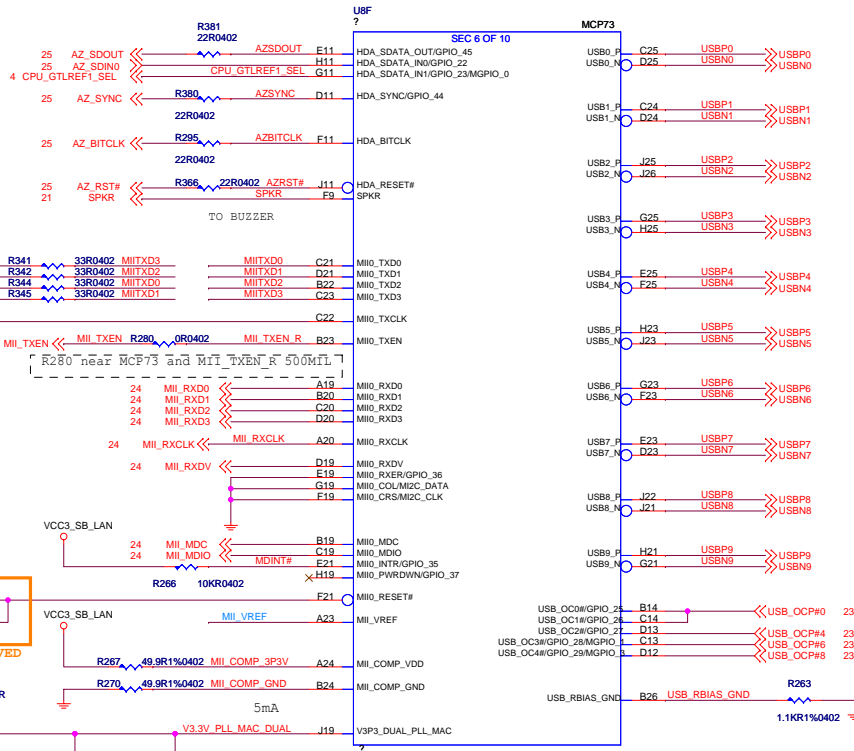
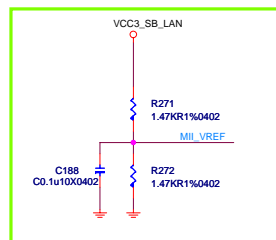
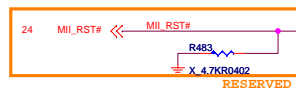
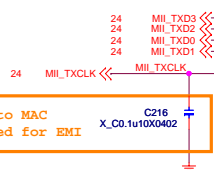
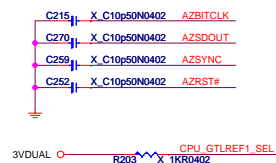
PLACE CAPS AT CONNECTOR.



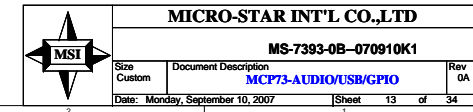
MICRO-STAR INT'L CO.,LTD

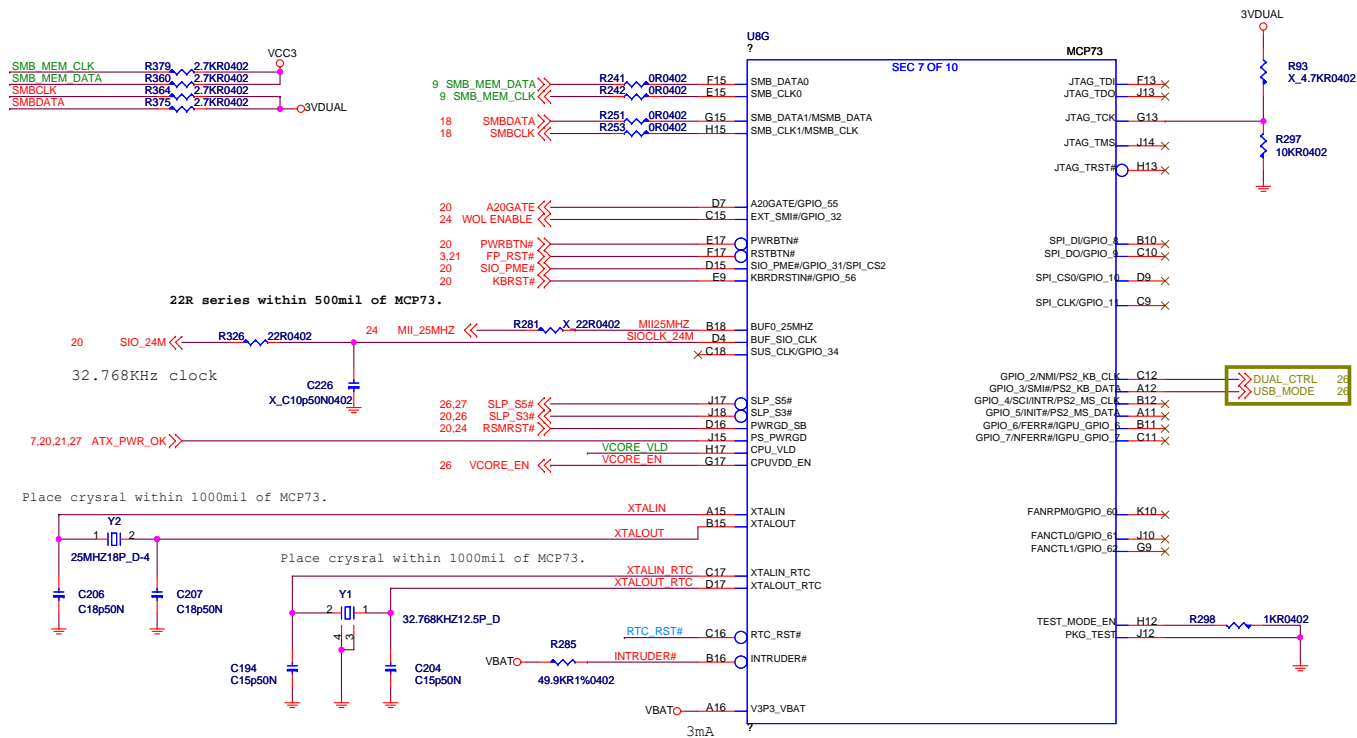
MS-7393-0B-070910K1

Size	Document Description	Rev
Custom	MCP73-SATA/IDE	0A
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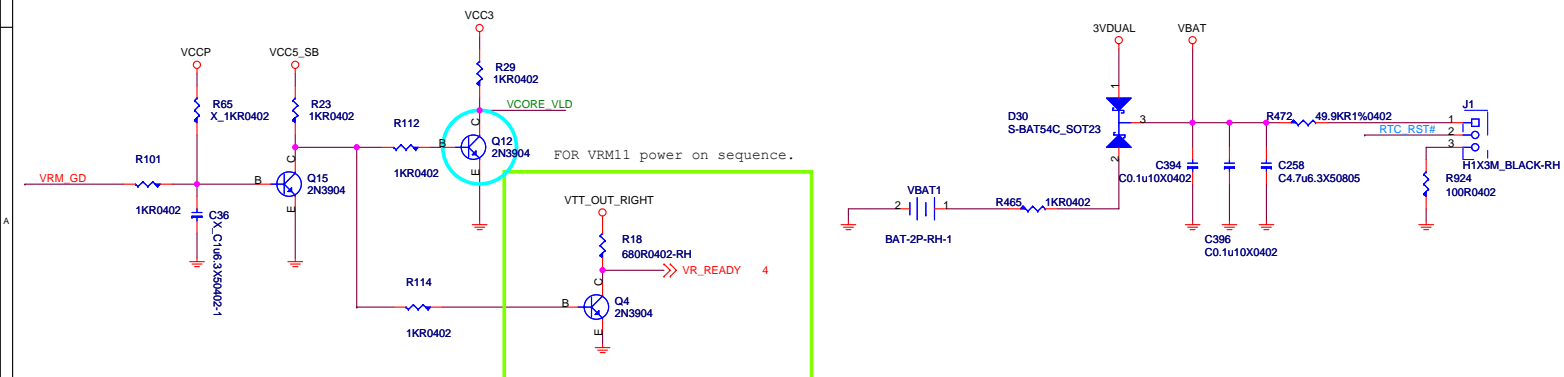


SPKR	0 = User Mode Boot Init table 1 = Safe Mode Boot Init table	Selects between a USER and initialization parameters. 10 k to GND : USER mode boot 10 k to +3.3V: SAFE mode boot
HDA_SYNC	0 = 14.31818 MHz 1 = 24 MHz	Selects the SIO clock to be either 14.31818 MHz or 24 MHz 10 k to GND: 14.31818 MHz 10 k to +3.3V: 24 MHz
HDA_RESET#	0 = MII 1 = RGMII	Selects between the MII and RGMII interface for MCF67 MAC 10 k to GND: MII 10 k to +3.3V_DUAL: RGMII
HDA_SDATA_OUT (MSB) LPC_FRAME# (LSB)	00 = LPC BIOS 01 = PCI BIOS 10 = SPI BIOS 11 = Reserved (SPI BIOS)	Select which bus the BIOS will be executed from 8.2 k to GND or 8.2 k to +3.3V
SPI_DO / GPIO_9 (MSB) SPI_CLK / GPIO_11 (LSB)	00 = 31 MHz 01 = 42 MHz 10 = 25 MHz 11 = 1 MHz	Selects the clock frequency for the SPI EEPROM 8.2 k to GND or 8.2 k to +3.3V_DUAL





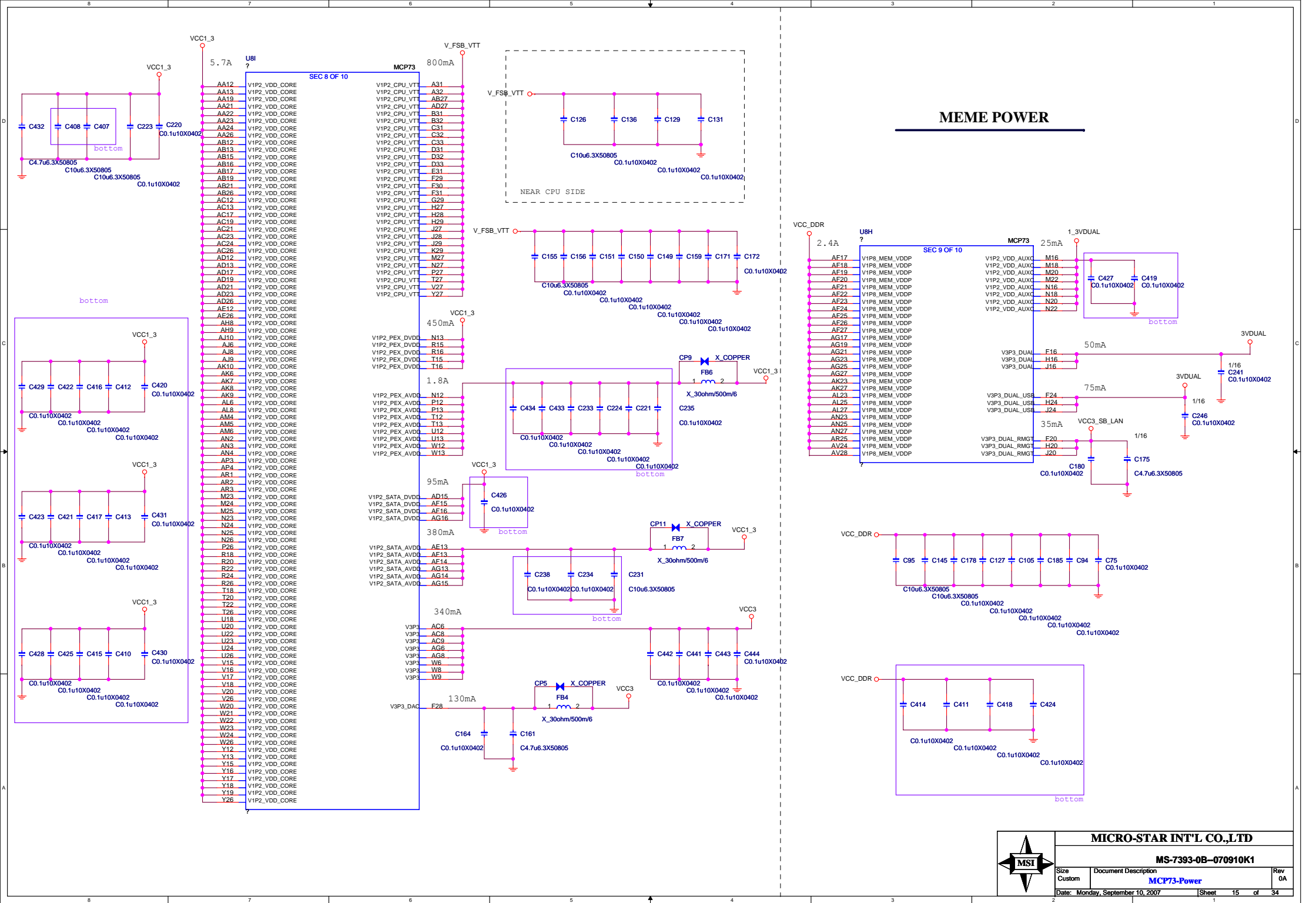
Vcore power-on sequence control circuit

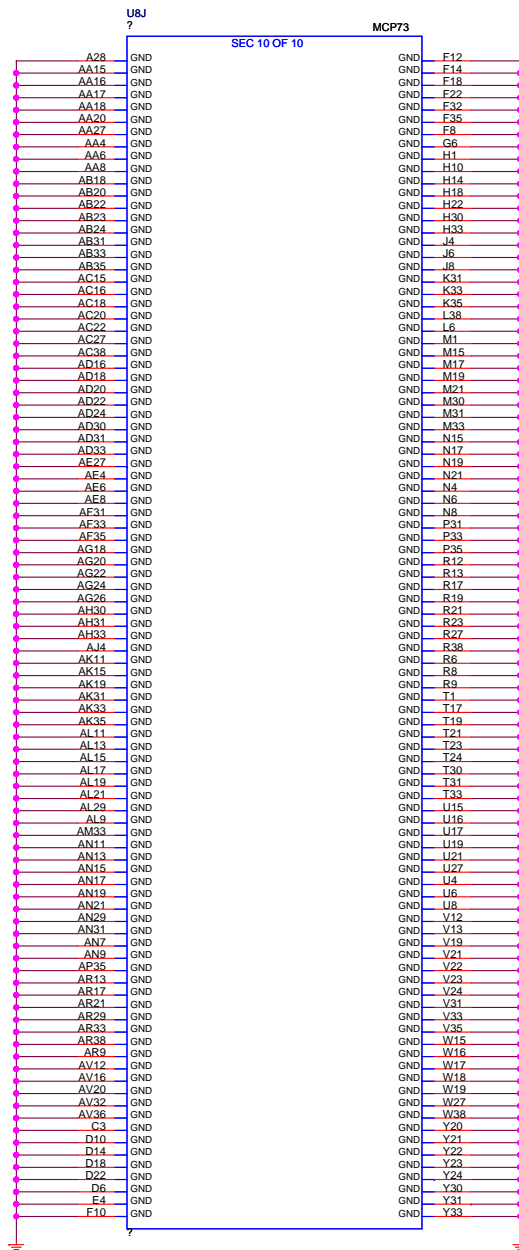


MICRO-STAR INT'L CO.,LTD

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Custom	MCP73-SPI/SMB	0A
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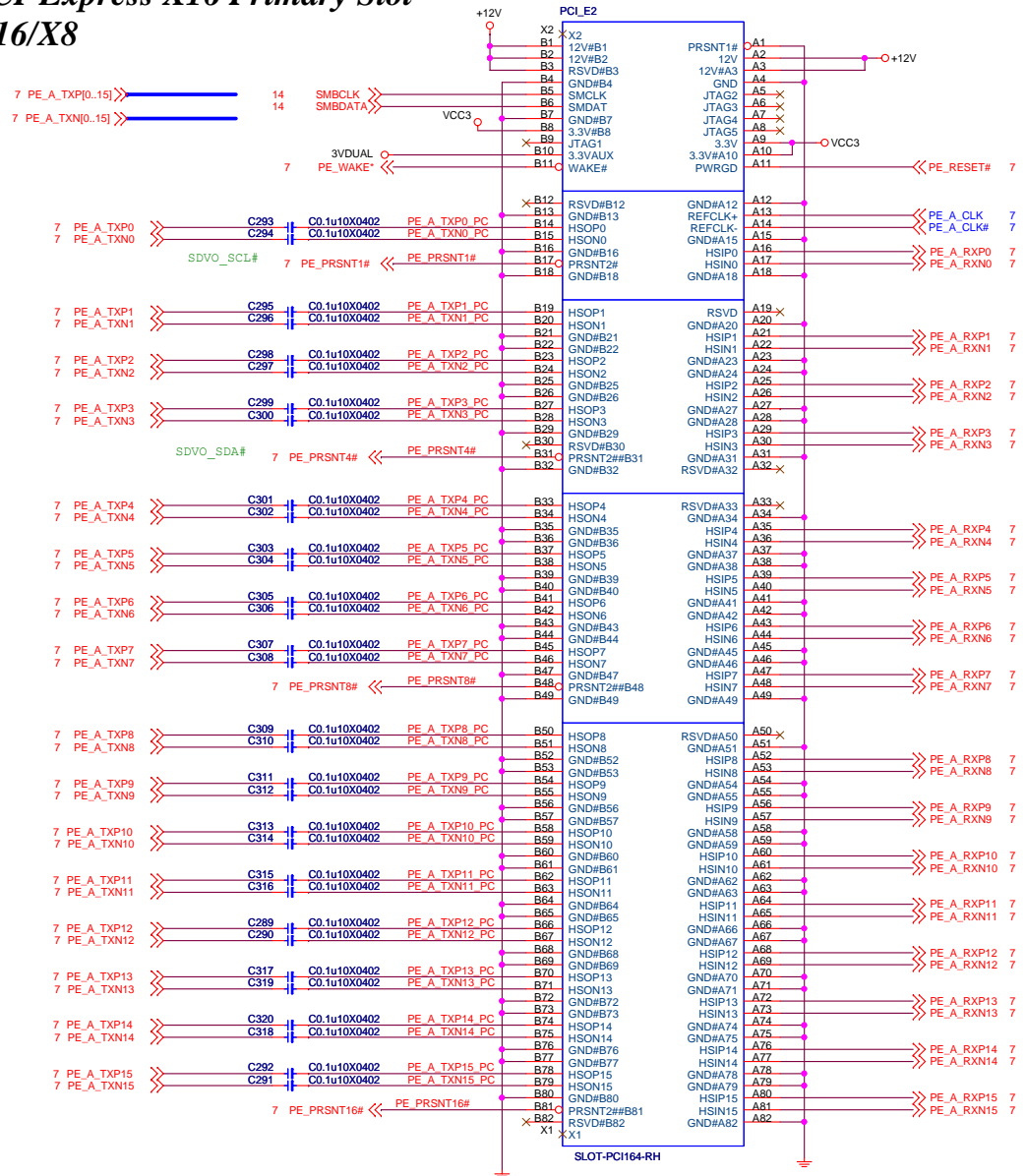


MICRO-STAR INT'L CO.,LTD

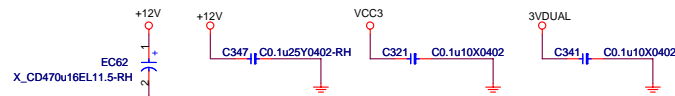
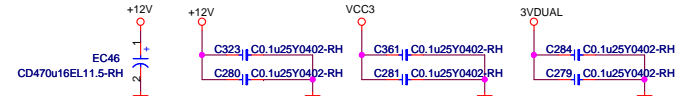
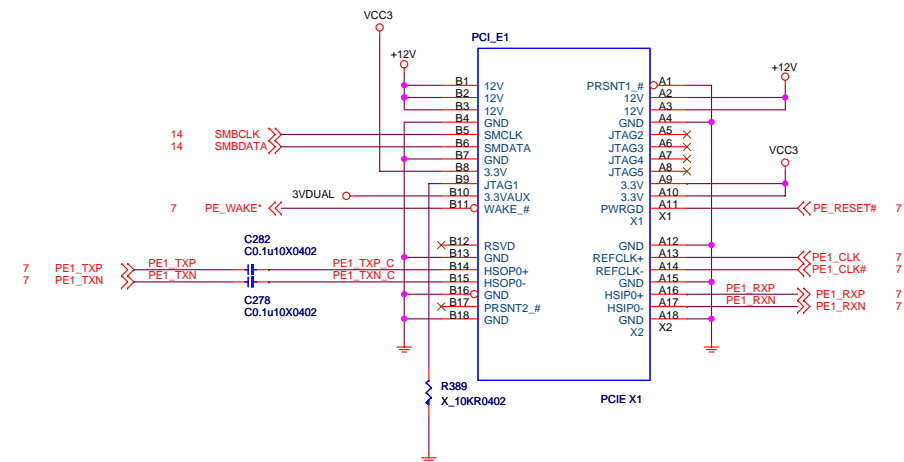
MS-7393-0B-070910K1

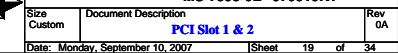
Size	Document Description	Rev
Custom	MCP73-GND	0A
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PCI-Express X16 Primary Slot X16/X8



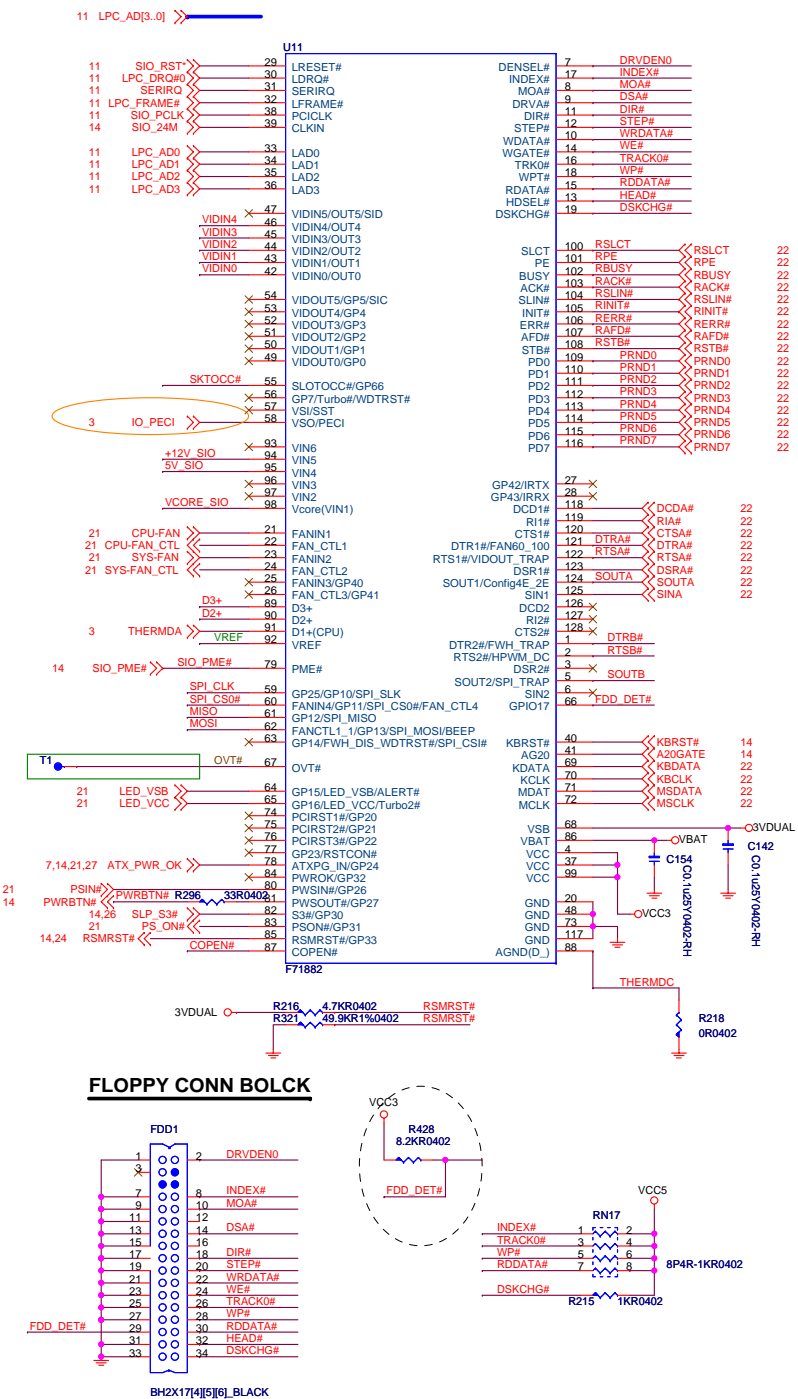
PCI-Express x1 SLOT 1





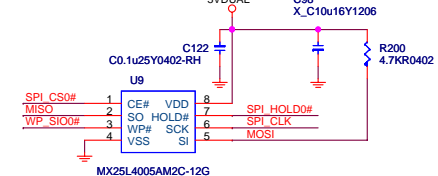
Super I/O

LPC SUPER I/O F71882



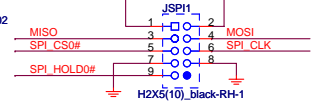
SPI 4M FLASH ROM

M31-25L4002-M24
M31-25X4003-W03

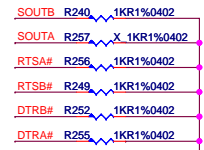


SPI DEBUG PORT

Part Number : N31-2051451-H06
Place close to SPI ROM



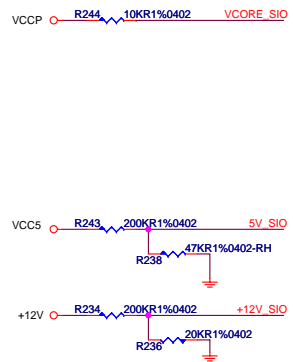
Strapping



	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT	PIN49-54=GPIO
	PIN42-47=VIDIN	PIN42-47=VIDIN/OUT
SOUTA	4E	2E
DTRB#, SOUTB	SPI_DISABLE	SPI_ENABLE
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%

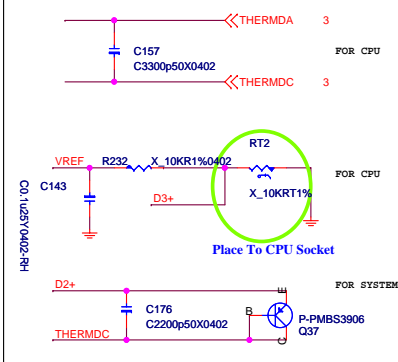
VOLTAGE SENSING(H/W Monitor).

The best voltage input level is about 1V.

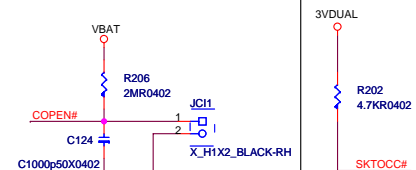


Temperature Sensing

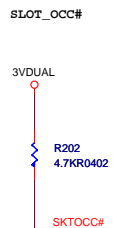
DIODE SENSING CIRCUIT



CASE OPEN CIRCUIT



CPU VID reset

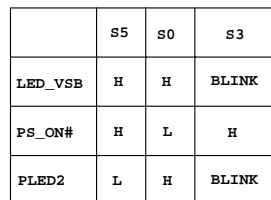


MICRO-STAR INT'L CO.,LTD

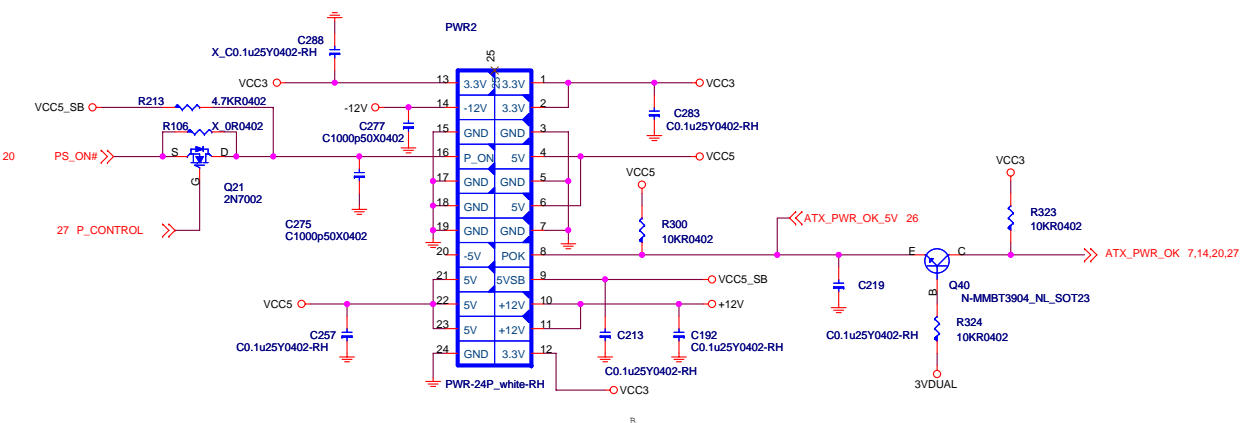
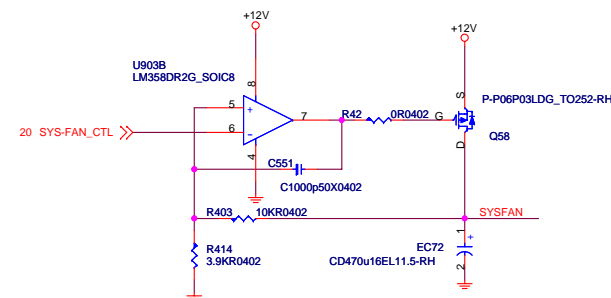
MS-7393-0B-070910K1

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Custom	LPC-Super I/O F71882FG	0A
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Intel Front Panel



ATX Connector

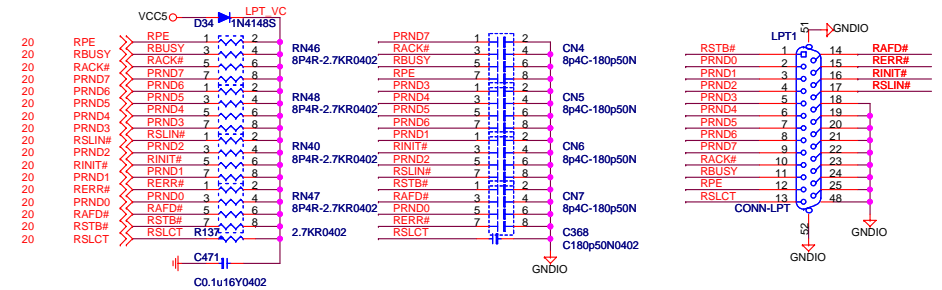
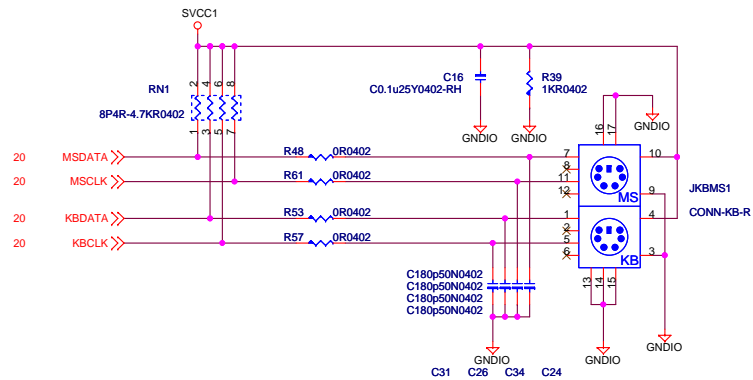
[illegible]

MICRO-STAR INT'L CO.,LTD

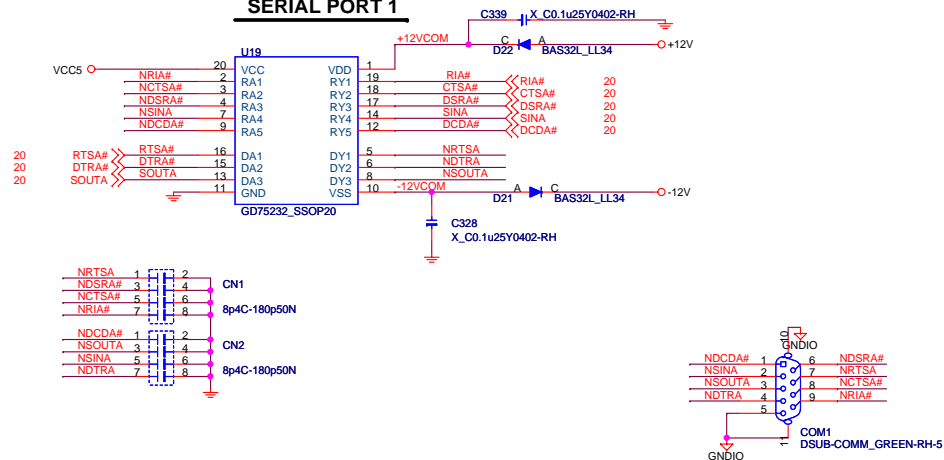
MS-7393-0B-070910K1

Size Custom	Document Description ATX/Front Panel/FAN	Rev 0A
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PS2 KEYBOARD & MOUSE CONNECTOR



SERIAL PORT 1



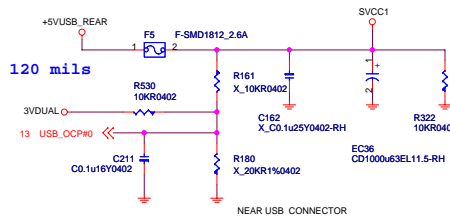
MICRO-STAR INT'L CO.,LTD

MS-7393-0B-070910K1

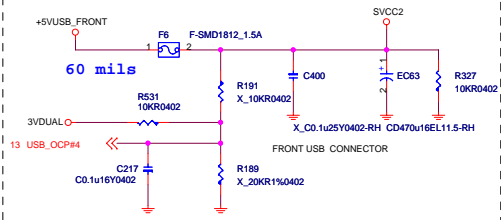
Size	Document Description
Custom	KB/COM1/IDE/FAN

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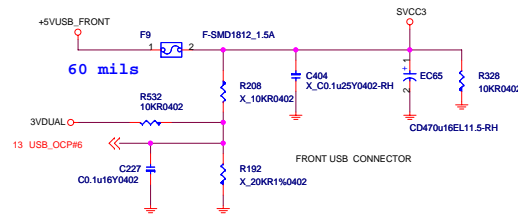
POWER CIRCUIT FOR USB PORT 0,1,2,3



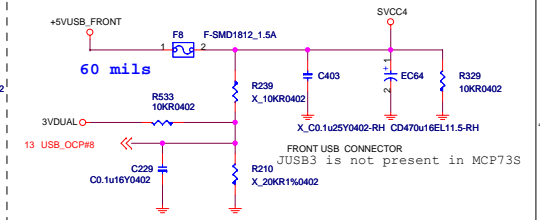
POWER CIRCUIT FOR USB PORT 4,5



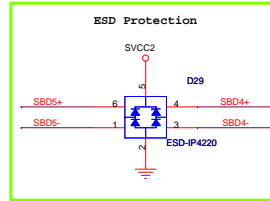
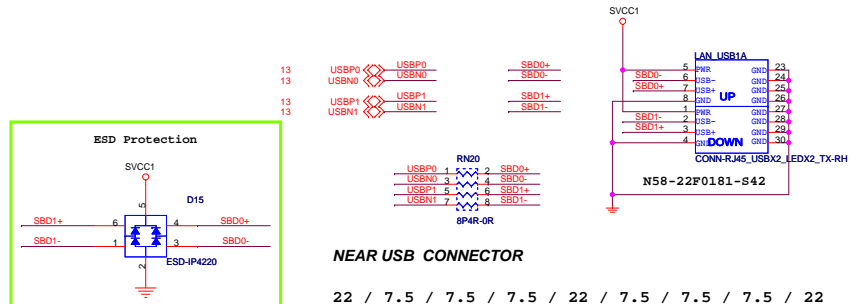
POWER CIRCUIT FOR USB PORT 6,7



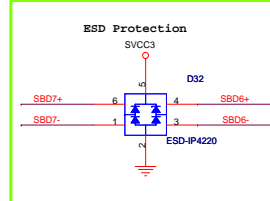
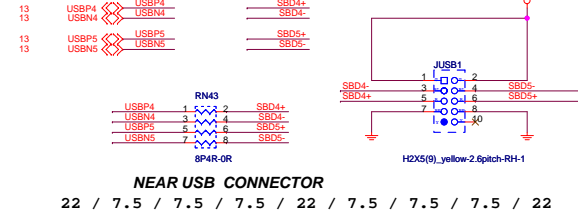
POWER CIRCUIT FOR USB PORT 8,9



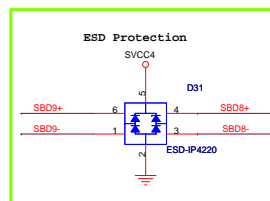
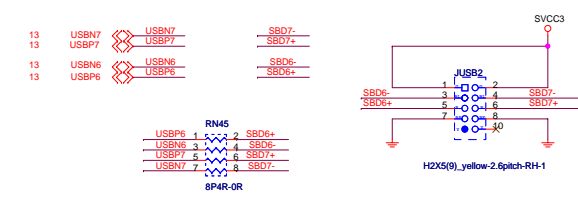
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



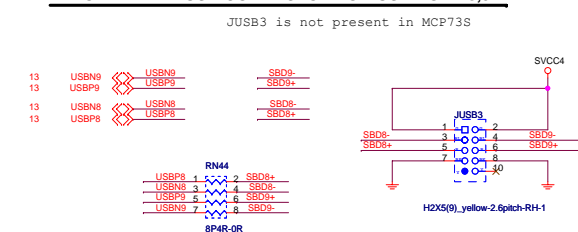
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



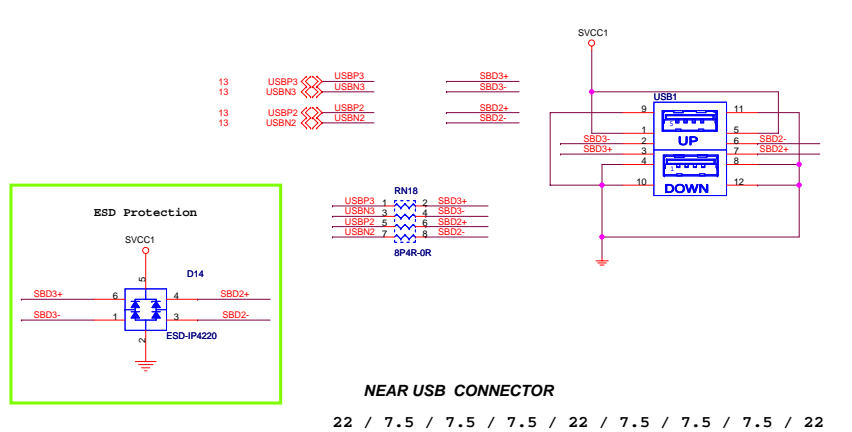
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

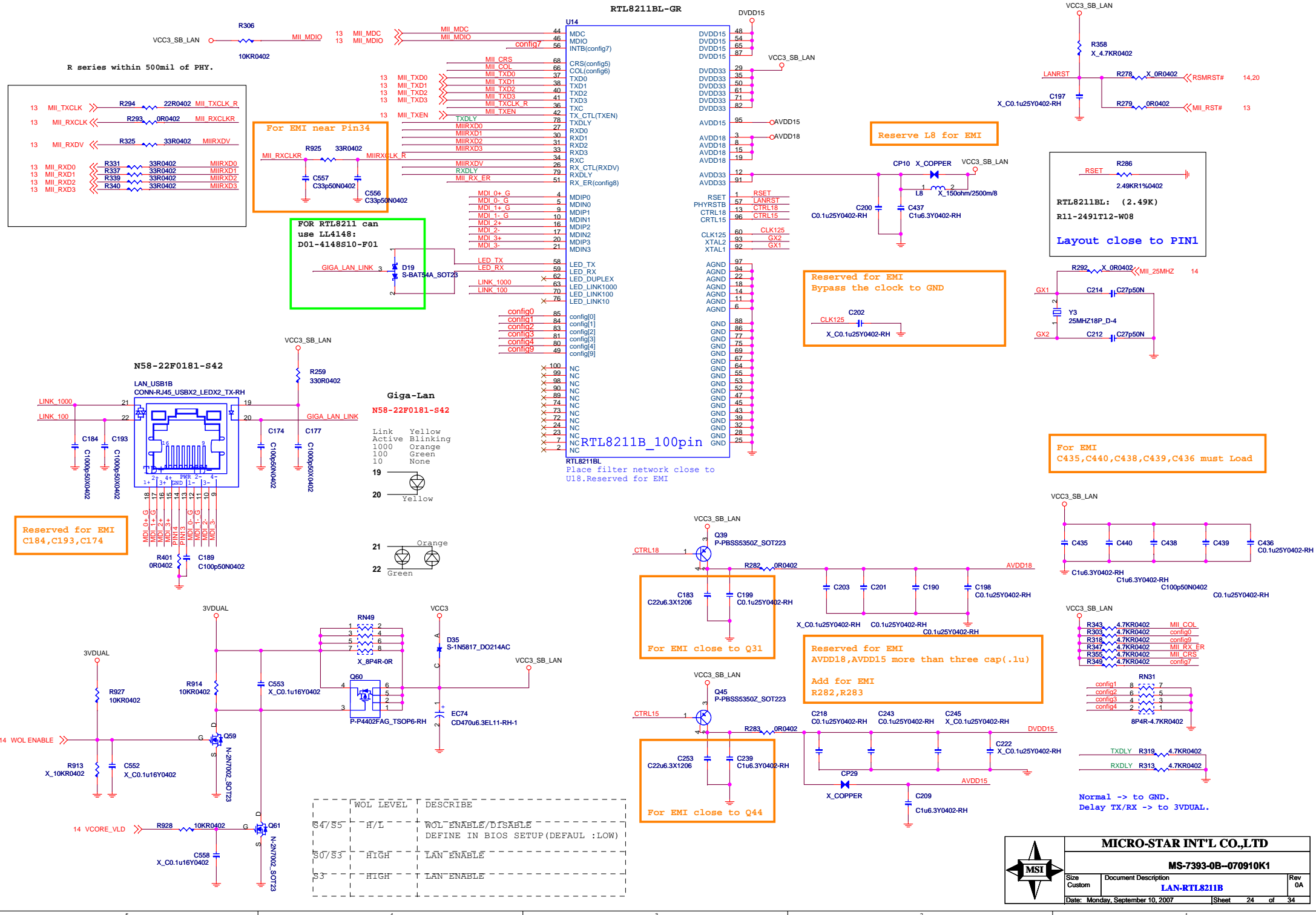


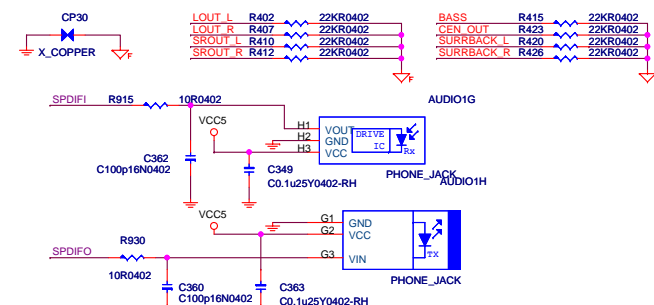
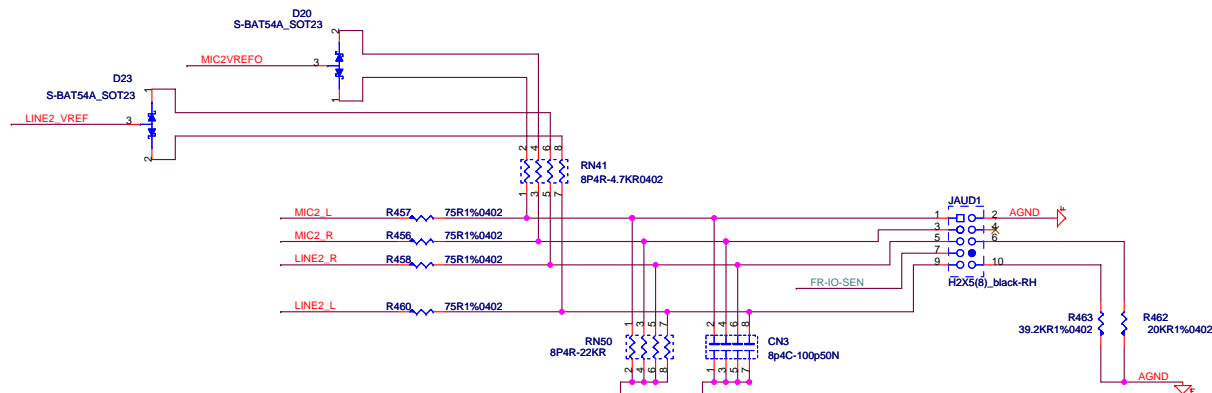
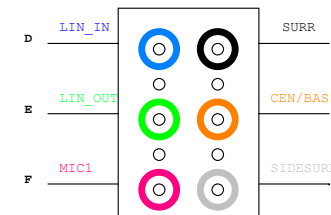
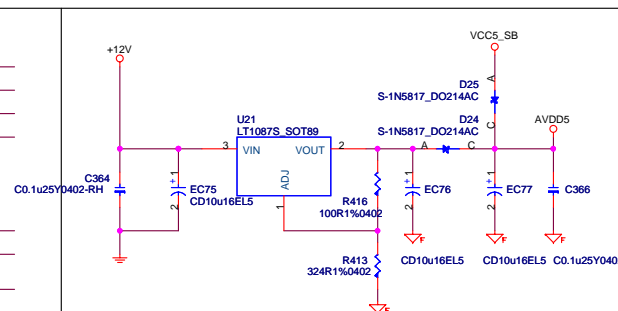
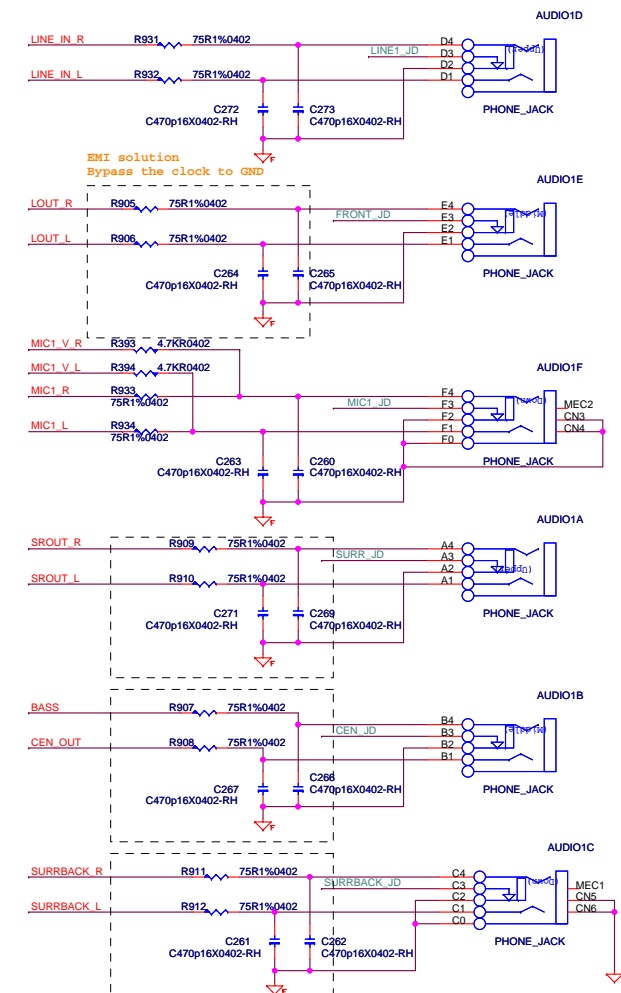
FRONT PANEL USB CONNECTOR FOR USB PORT 8,9



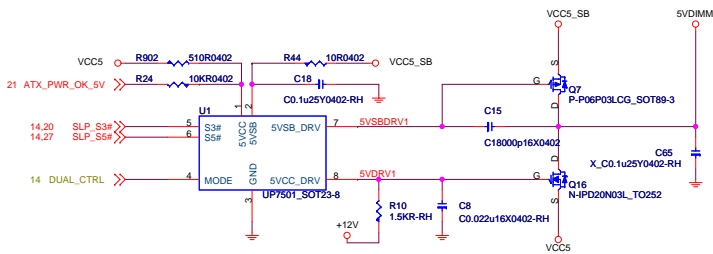
REAR PANEL USB CONNECTOR FOR USB PORT 2,3





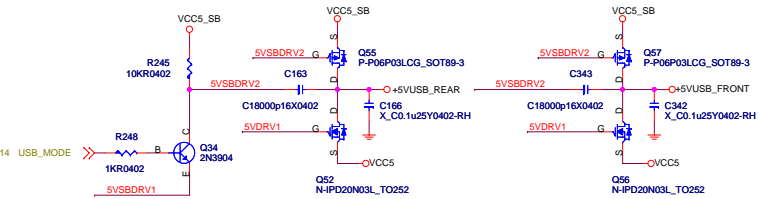


5VDIMM FOR DDR

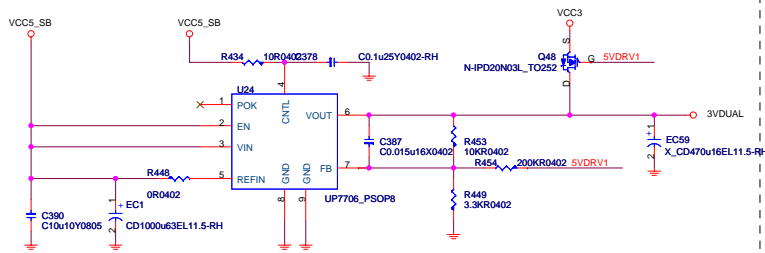


5VSB FOR Rear USB

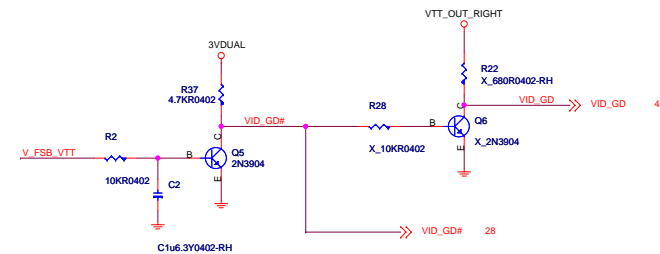
5VSB FOR Front USB



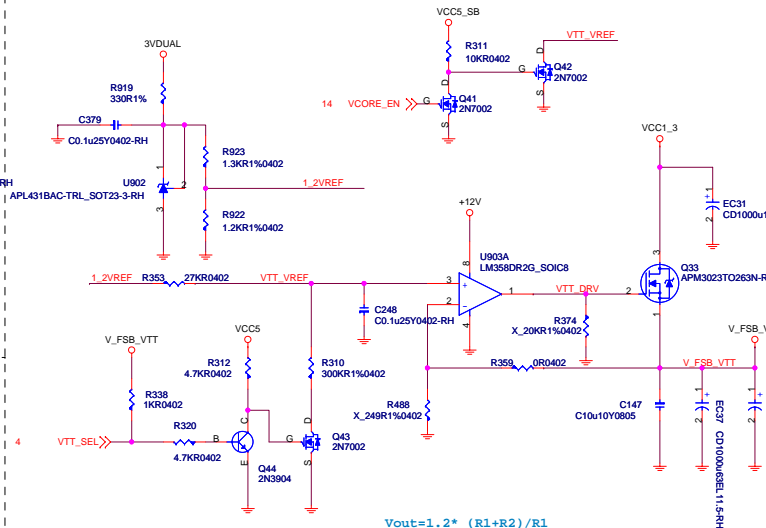
3VDUAL, ?A



VID_GD# to PWM and VID_GD to CPU for VRM10 power sequence.

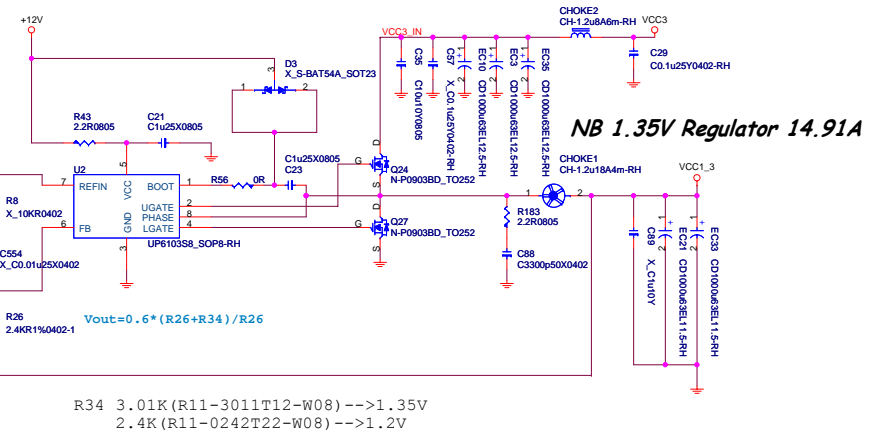


V_FSB_VTT



VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

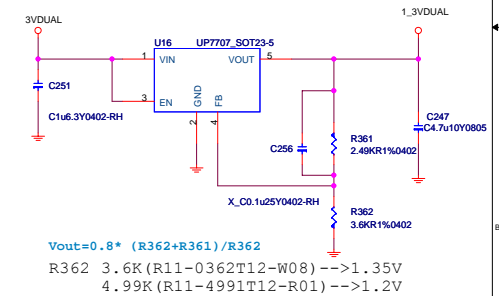
$$V_{out} = 1.2 * (R1 + R2) / R1$$



$$R34 \ 3.01K (R11-3011T12-W08) \rightarrow 1.35V$$

$$2.4K (R11-0242T22-W08) \rightarrow 1.2V$$

1_3VDUAL, 25mA



$$V_{out} = 0.8 * (R362 + R361) / R362$$

$$R362 \ 3.6K (R11-0362T12-W08) \rightarrow 1.35V$$

$$4.99K (R11-4991T12-R01) \rightarrow 1.2V$$

	S0	S3	S4	S5
DUAL_CTRL	X	X	0	1
5VSBDRV1	1	0	1	0
5VDRV1	1	0	0	0
5VSBDRV2	X	0	1	0
USB_MODE	X	1	X	1
5VDIMM	Y	Y	N	Y
USB power	Y	Y	N	Y



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Custom	ACPI Controller	0A

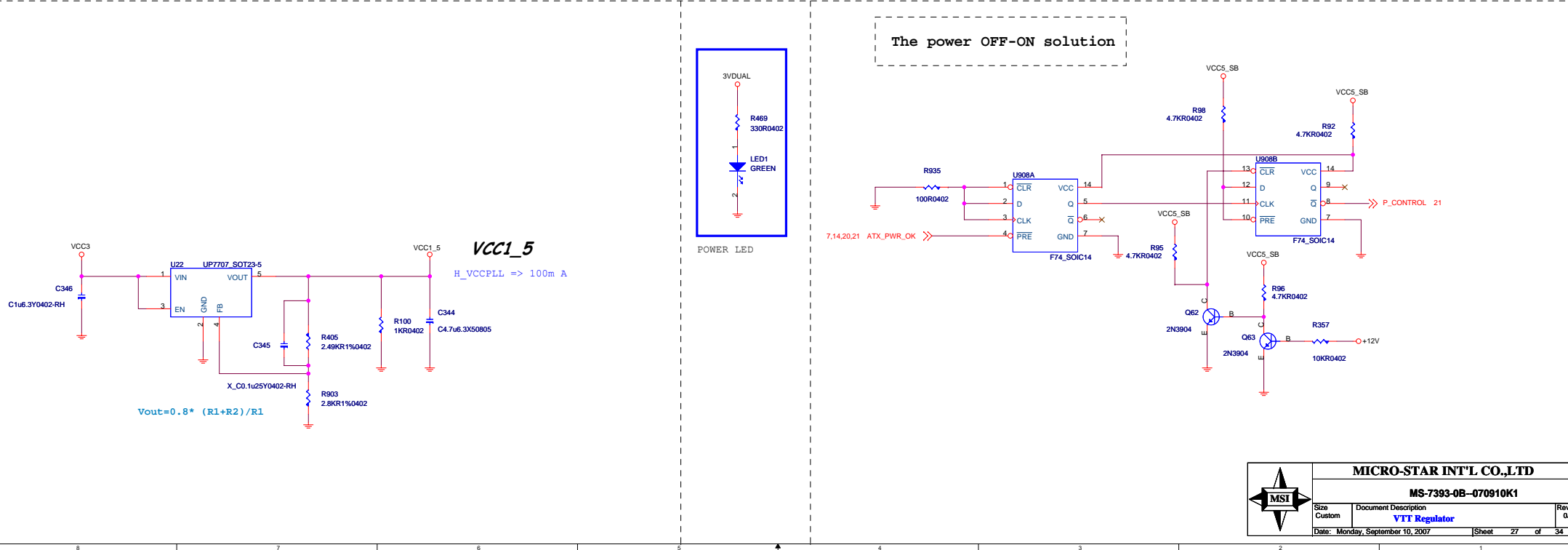
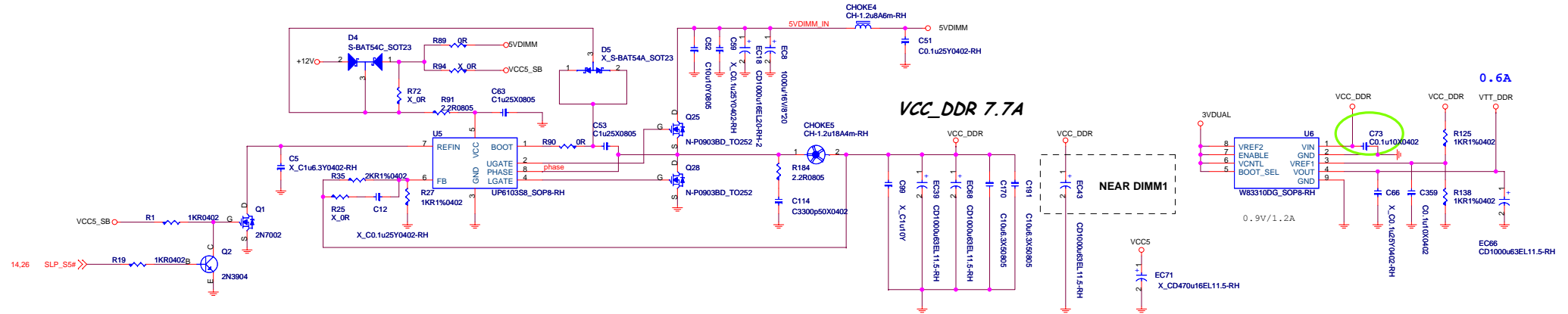
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DDR II 1.8V POWER

$$\begin{aligned} \text{Iripple} &= 7.7 \times 0.6 \times 0.8 / 1 = 3.70\text{A} \\ 2.35 \times 2 \times 1.7 &= 7.99 > 3.70\text{A} \end{aligned}$$

VTT_DDR

To CPU Copper trace width > 200mils

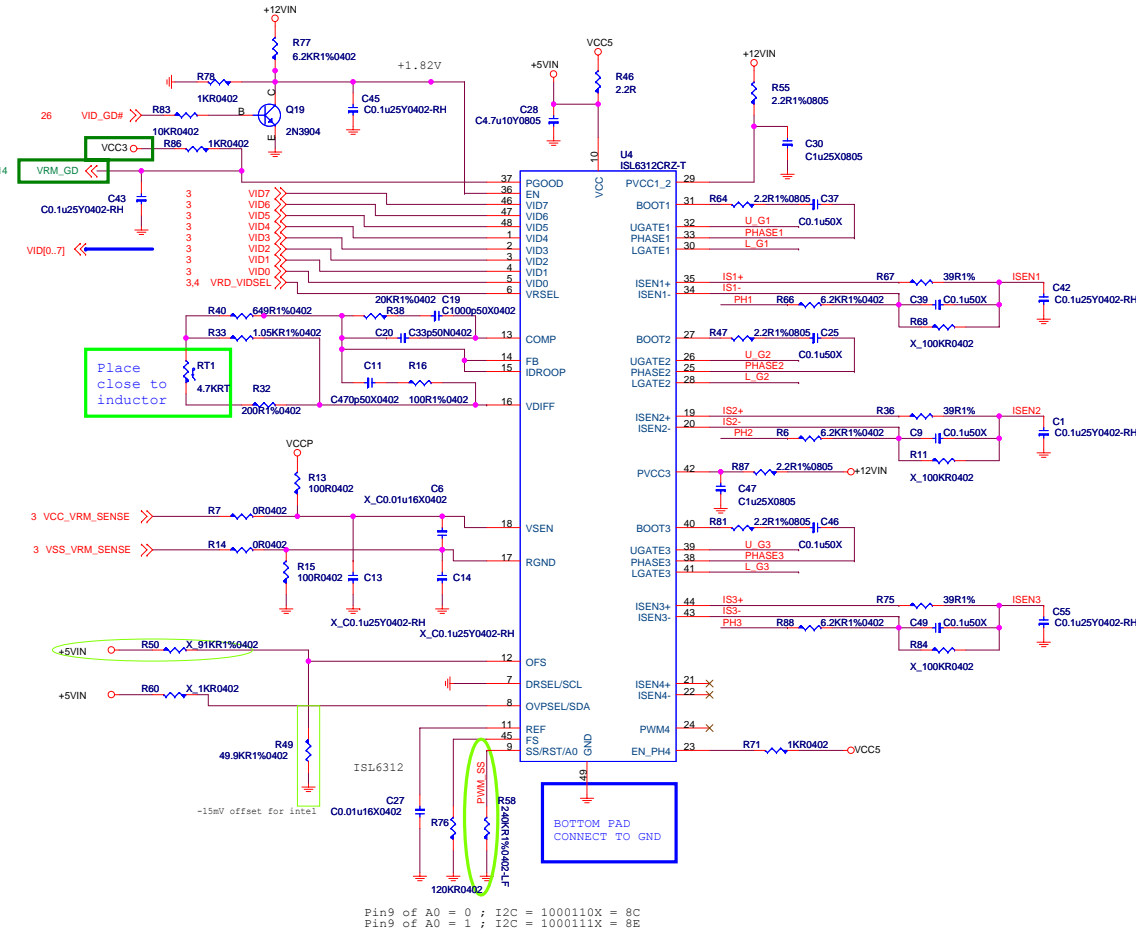


The power OFF-ON solution

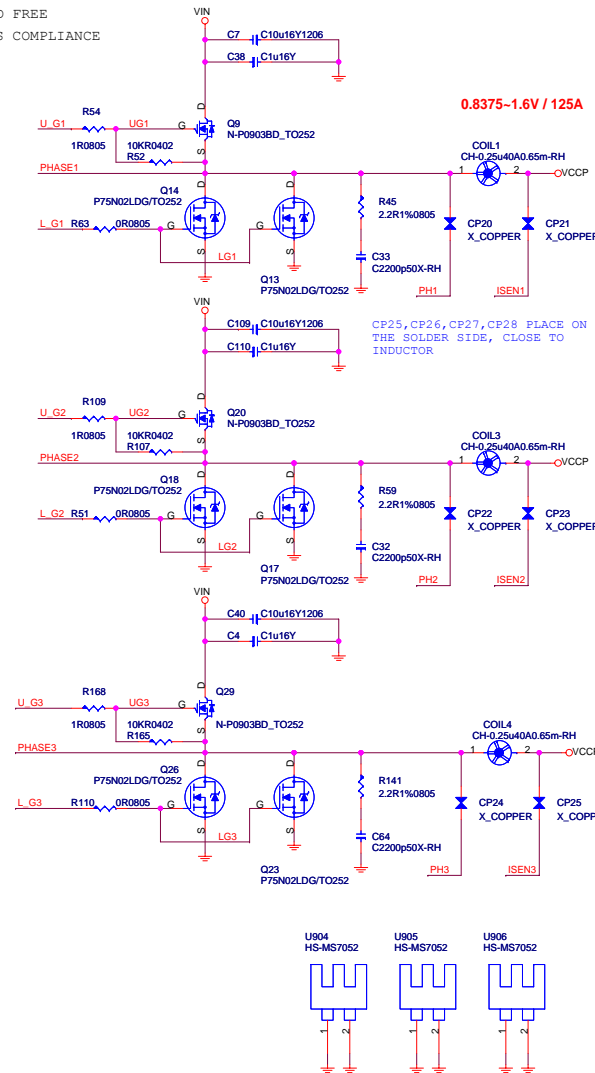
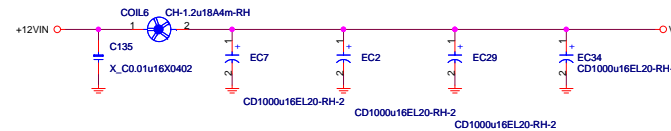
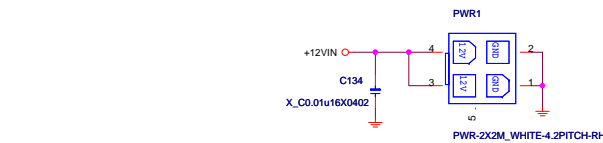
Voltage Regular Module

N-P0903BDG_TO252
P75N02LDG/TO252
C100U2SP
CD560U40S-2
1800UF/6.3V
0.25uH/40A
CH-1.1U25A-LF
CD1000U16EL20-2

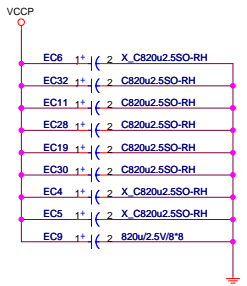
mosfet/n-channel, P0903BDG, SMT/TO252, Rds(on)=9.5mΩ(10V/25A), Vgs(on)=1~3V, Id=50A, Ciss=1800pF, Qg=50nC, Vds=25V, Vgs=±20V, RoHS compliance
mosfet/n-channel, P75N02LDG, SMT/TO252, Rds(on)=7mΩ(10V, 30A), Vgs(on)=1~3V, Id=75A, Ciss=5000pF, Qg=140nC, Vds=25V, Vgs=±20V, RoHS compliance
ESR<13mΩ, Ripple cur.<2.7A, LC<12uA, 105C
CAP, OS-CON, 560u/4V, Dip-2/8*9/3.5mm, ESR<7mohm, Ripplecur.=6100mA, Lc. <500uA, SPEC series, RoHS compliance
ESR<12mΩ, Ripplecur<2350mA, 105C, longlife change from 2000hrs to 3000hrs, KZJ series
, IND CHOKE, 0.25uH, 20%, DIP/8.5mm, 40A, 0.6mOhm, , PEW, FERRITE, SQUARE, RoHS COMPLIANCE
IND CHOKE, 1.1uH, 20%, DIP/9mm, 25A, 1.4mOhm, 5.5T, 0.9mmx3, PEW, IRON, , LEAD FREE
CAP, EL, 1000u, 16V, Dip-8x20/3.5mm, 20%, 12mOhm, 2350mA, 105C, 3000hrs, RoHS COMPLIANCE



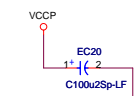
Pin9 of A0 = 0 ; I2C = 1000110X = 8C
Pin9 of A0 = 1 ; I2C = 1000111X = 8E



OS-CON Capacitors

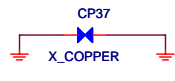
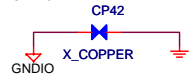
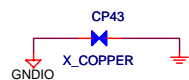
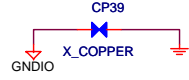
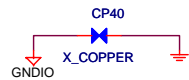
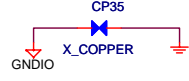
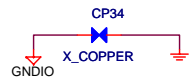
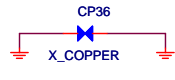
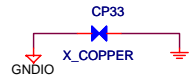
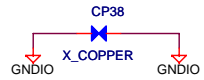
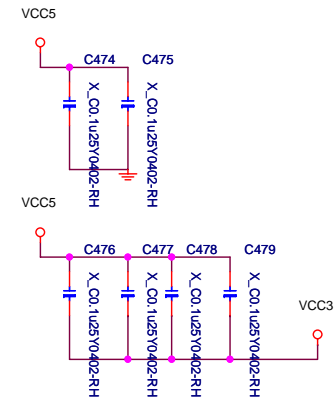
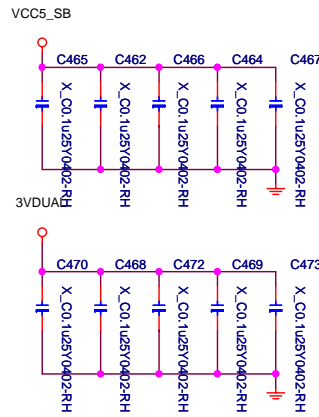
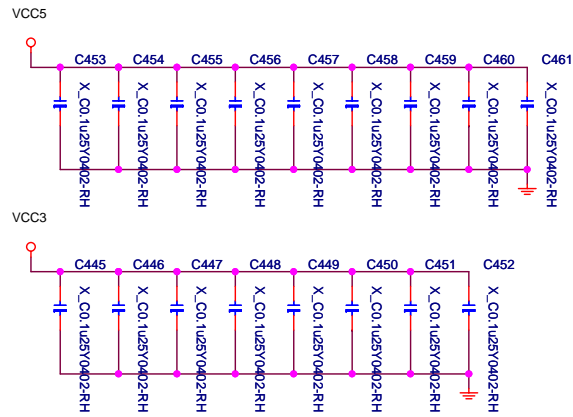


SP Capacitors

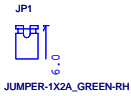
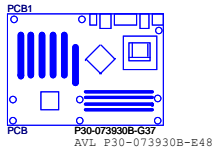
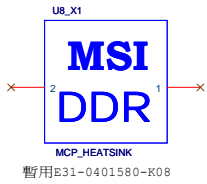


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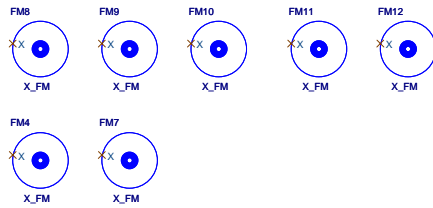
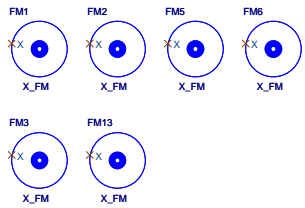
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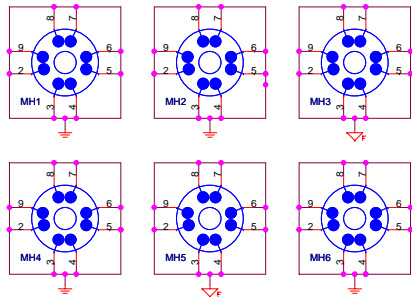
Title		
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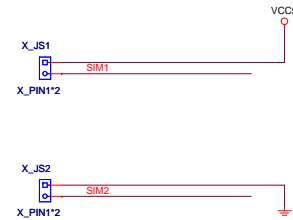
Optics Orientation Holes



Mounting Holes



Simulation



MCP73 GPIO Config.

Contol Register	Primary Signal	Secondary Function	Tertiary Funtion	Default State
C1	GPIO_2	NMI	PS2_CLK0	GPIO Input
C2	GPIO_3	SMI #	PS2_DATA0	GPIO Input
C3	GPIO_4	SCI/INTR	PS2_CLK1	GPIO Input
C4	GPIO_5	INT#	PS2_DATA1	GPIO Input
C5	GPIO_6	FERR#/SYS_SERR#	IGPU_GPIO_6	GPIO Input
C6	GPIO_7	NFERR#/SYS_PERR#	IGPU_GPIO_7	GPIO Input
C7	GPIO_8		SPI_DI	Tertiary Function
C8	GPIO_9		SPI_DO	Tertiary Function
C9	GPIO_10		SPI_CS0	Tertiary Function
CA	GPIO_11		SPI_CLK	Tertiary Function
D2	LPC_DRQ1#	GPIO_19	FANRPM1	GPIO Input
D3	PROCHOT#	GPIO_20		Primary Function
D4	PE_WAKE#	GPIO_21		Primary Function
D5	HDA_SDATA_IN0	GPIO_22		Primary Function
D6	HDA_SDATA_IN1	GPIO_23	MGPIO_0	Primary Function
D7	HDA_SDATA_IN2	GPIO_24	MGPIO_2	Primary Function
D8	USB_OC0#	GPIO_25		Primary Function
D9	USB_OC1#	GPIO_26		Primary Function
DA	USB_OC2#	GPIO_27		Primary Function
DB	USB_OC3#	GPIO_28	MGPIO_1	Primary Function
DC	USB_OC4#	GPIO_29	MGPIO_3	Primary Function
DD	PCI_PME#	GPIO_30		Primary Function
DE	SIO_PME#	GPIO_31	SPI_CS2	Primary Function
DF	EXT_SMI#	GPIO_32		Primary Function
E1	SUS_CLK	GPIO_34		Primary Function
E2	MII0_INTR	GPIO_35	PWR_LED#	Primary Function
E3	MII0_RXER	GPIO_36		Primary Function
E4	MII0_PWRDWN	GPIO_37		Primary Function
E5	PCI_REQ3#	GPIO_38	RS232_CTS#	GPIO Input
E6	PCI_GNT3#	GPIO_39	RS232_RTS#	GPIO Output High
E7	PCI_REQ2#	GPIO_40	RS232_DSR#	GPIO Input
E8	PCI_GNT2#	GPIO_41	RS232_DTR#	GPIO Output High
E9	PCI_CLKRUN#	GPIO_42		Primary Function
EA	PCI_PERR#	GPIO_43	RS232_DCD#	GPIO Input
EB	HDA_SYNC	GPIO_44		Primary Function
EC	HDA_SDATA_OUT	GPIO_45		Primary Function
F1	LPC_DRQ0#	GPIO_50		Primary Function
F3	PCI_REQ4#	GPIO_52	RS232_SIN#	GPIO Input
F4	PCI_GNT4#	GPIO_53	RS232_SOUT#	GPIO Output High
F6	A20GATE	GPIO_55		Primary Function
F7	KBRDSTIN#	GPIO_56		Primary Function
F8	SATA_LED#	GPIO_57		Primary Function
F9	THERMTRIP	GPIO_58		Primary Function
FA	THERM#	GPIO_59		Primary Function
FB	FANRPM0	GPIO_60		Primary Function
FC	FANCTL0	GPIO_61		Primary Function
FD	FANCTL1	GPIO_62		Primary Function
FE	CABLE_DET_P	GPIO_63		Primary Function

PCI Config.

DEVICE	MCP1 INT Pin	REQ# /GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTA* PCI_INTB* PCI_INTC* PCI_INTA*	PCI1REQ* PCI1GNT*	AD22	PCICLK_SLOT1
PCI Slot 2	PCI_INTB* PCI_INTC* PCI_INTD* PCI_INTA*	PCI2REQ* PCI2GNT*	AD23	PCICLK_SLOT2

DDRII DIMM Config.

DIMM1	DIMM2
A0 1010000B	A2 1010001B
0A	1A

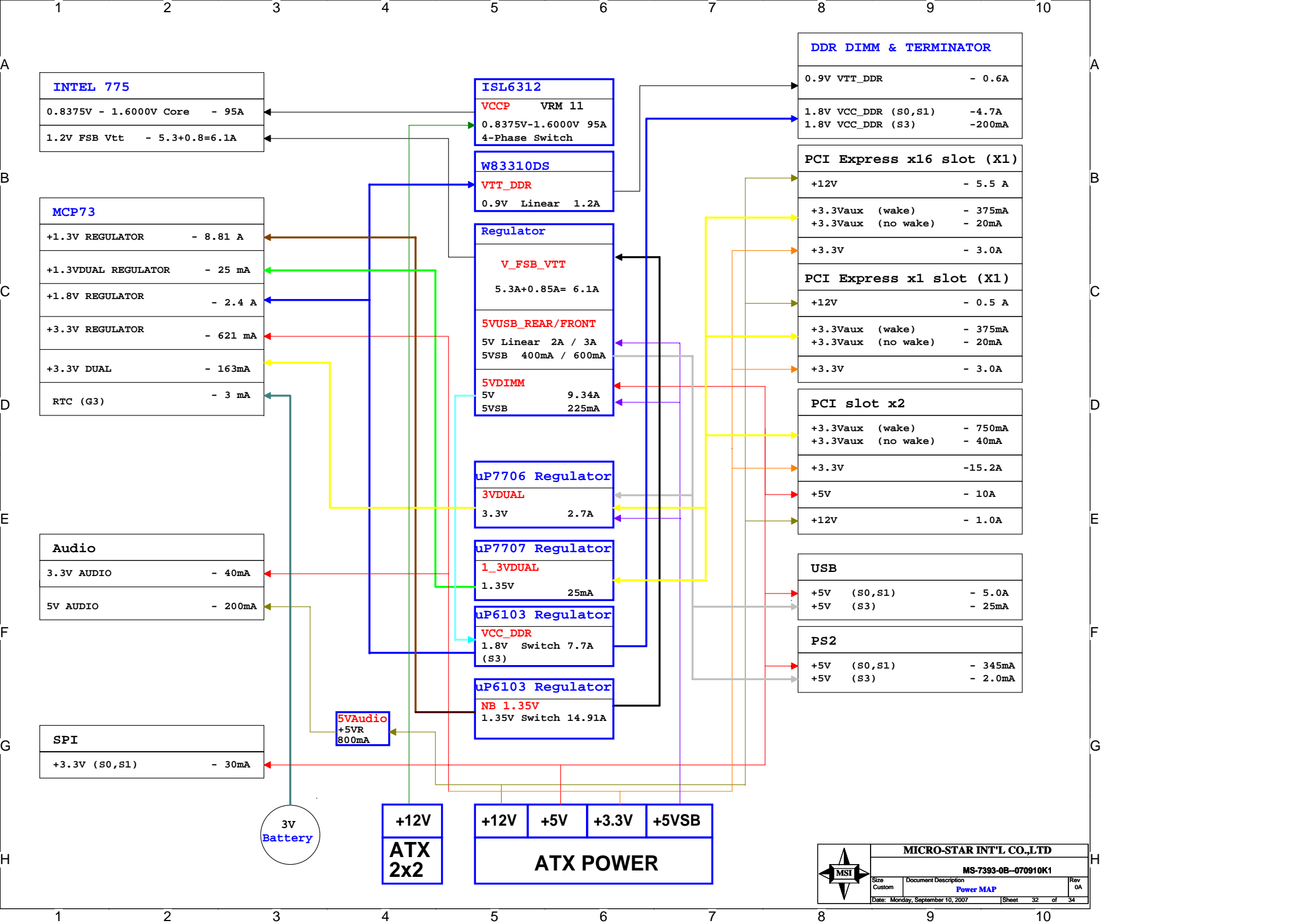
SIO GPIO FUNCTION

NAME	Function Description
FANIN1	CPU-FAN
FAN_CTL1	CPU-FAN_CTL
FANIN2	SYS-FAN
FAN_CTL2	SYS-FAN_CTL
FANIN3	NB-FAN

MCP73 GPIO FUNCTION

NAME	Function Description
GPIO_2	DUAL_CTRL
GPIO_3	USB_MODE
GPIO_23	CPU_GTLREF1_SEL



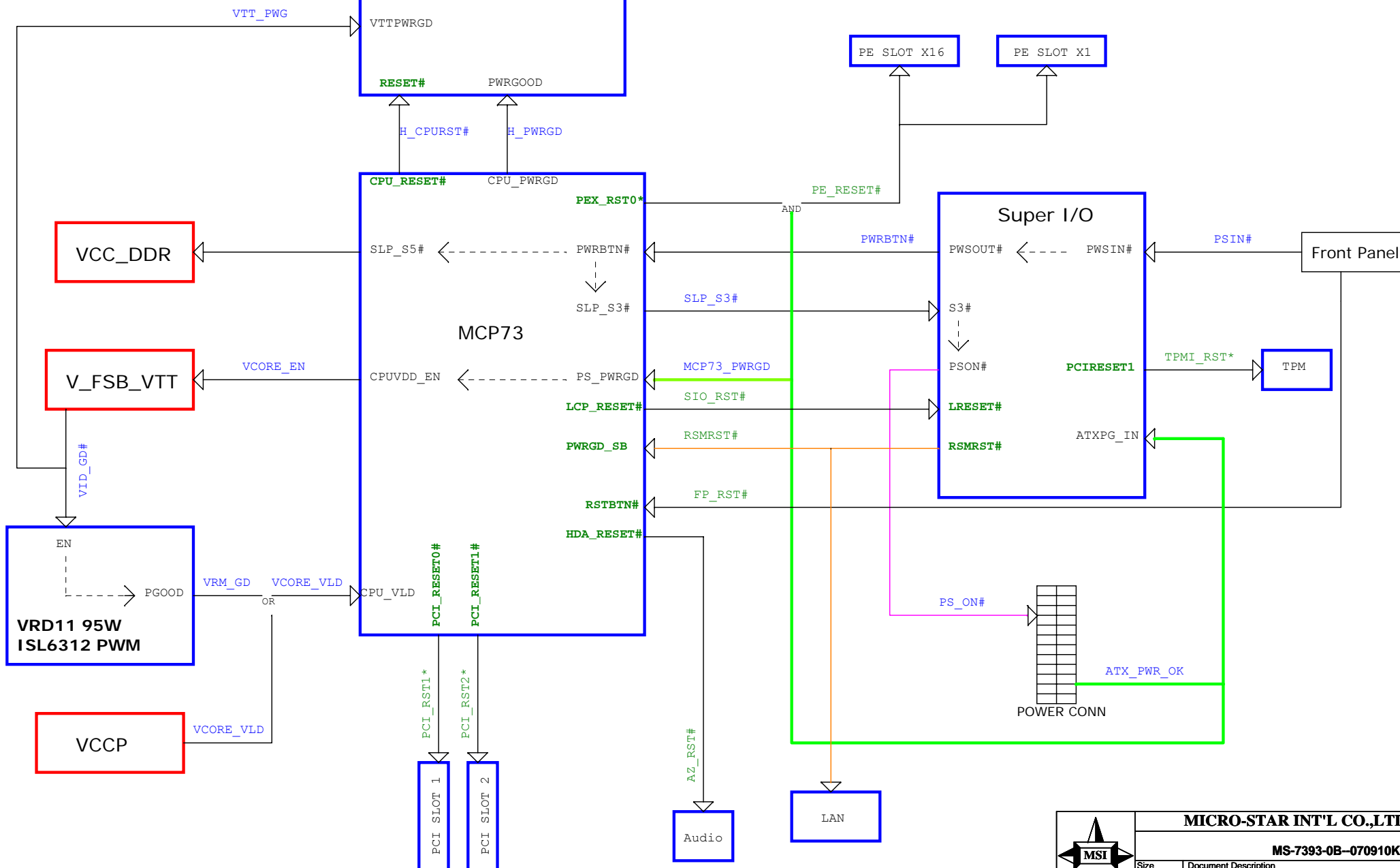


PWROK MAP

INTEL P4 LGA775

VTT_PWG → VTPWRGD

RESET# PWRGOOD




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Ver.	Date	Change List	Page	Ver.	Date	Change List	Page
0A	2007.0604	1.Add MCP73 strap option table in schematic	13	0B	2007.0801	18.Modify R404 from 22k to 10Kohm, Nvidia confirm	07
		2.Add standby LED	27			19.RGMII MAC interface	13,24
		3.Add GPIO table in schematic	31			Page.13 pin E19,G19,F19 to GND	
		4.Add FDD detect function on pin29 of FDD connector	20			Page.24 Modify R293 from 22 to 0 ohm	
		5.Add SPDIF in/out	25			20.Realtek Lan Current update	24
		6.Critical de-caps should be X7R type				Reserve R358,C203,C222,C216	
		7.GTLREF1 value in schematic it has been changed.	04			Modify C183,C253 from 10 u to 22u	
		8.LGE want to adopt 1W under in standby mode.	24			Add R282,R283	
		9.Need pull up resistor when not used.	23			21.Unload R936, R937, R938, R939	10
		10.TDI and TMS pull up to VCC,TRST pull down to GND	19			22.Unload R145,R158,R157 for Nvidia release VIL	04
		11.Add 22ohm resistor near PHY of MII_TXCLK, RXCLK	24			23.Add 0 ohm(R280) within MCP73	13
		12.SMB_DATA0,1, CLOCK0,1 reserve 0 ohm resistor near MCP73	14			24.Remove NB FAN	21
		13.AZ_RST reserve 10pF cap for AZ_RST	13			25.Unload R152 for Nvidia release	04
		14.VIP8_MEM_VDDP need 2 X 10uF (not 1uF)	27			26.Add C379	26
		15.PS_PWRGD (RSMRST#) pull down to GND	20			27.For Power Conconsumption	13,15,24
		16.Connect PECTI to Super I/O	03			Co-lay design 3VDUAL and VCC3_SB_LAN	
		17. it can be leakage path of VCC5_SB to VCC5.	21			28.For Nvidia release for VGA solution	17
		18.Add ESD protection as MS-7372	21			C112,C111,C120 change from 22P to 5.6P	
		19.LG want to unify reau audio color as MS-7372 and MS-7342	25			C102,C104,C115 change from 10P to 5.6P	
0B	2007.0801	20.Add VSYNC, HSYNC signals need 3.3V to 5V buffer.	17			L9,L10,L11 change from 68n to 100n	
		1.VCC3_SB_LAN change to 3vdual (change to item 27)	13			C69,C70 from unload 47P to load 12P	
		2.Nvidia release	06			29.Unload R292,R281	24
		R226,225,222,224 from 330hm to 0 Ohm ;				Load C214,C212,Y3	
		R219,214,152,148,223,221 unload					
		3.Nvidia release	04				
		Modify R209 from 62 Ohm to 200 Ohm					
		4.Some SMPS do not work when quick AC ON/OFF solution	27				
		5.The SIO pin LED_VCC can't work in S3 state, so we use	21				
		the pin LED_VSB and PS_ON# to control the Power					
		LED	20				
		6.Load R249 for linier FAN					
		7.Nvidia release	14				
		JTAG_TCLK pull high to 3.3dual(R93)					
		chip A02 cover it, so pull low(R297).					
		8.VRM Modify	28				
		ChangeR33 => 1.05k,R40 => 649R,R38 => 20k,					
		R16 => 100R,R6 ` R66 ` R88 => 6.2k,C11 => 470pF,					
		C19 => 1nF,C20 => 33pF					
		Remove EC4 ` EC5 ` EC6 => N/C					
		9.For VTT_PWG rise time keep <150ns solution	04.14				
		(DA-03414-001_v01.pdf)					
		P4. VTT_PWRGOOD area					
		P14. Vcore power-on sequence control circuit					
		10.Nvidia release(DA-02879-001_v02.pdf)	04				
		CPU_GTLREF1 modify					
		11.R324 pull-high from 5VSB to 3VDUAL	21				
		12.C22 modify from 10u to EC67 100u; R30 from 00hm to 2000hm;	21				
		Load D41,D2					
		13.Modify D16,D18 pull-high from 3VDUAL to VCC3	09				
		14.RGB solution load C112,C111,C120 22p	17				
		15.Unuse HDMI pull-high 10K(R390) to VCC3	07				
		16.Nvidia release	12				
		IDE_COMP_3P3V add .1u(C190) to GND					
		17.Nvidia release	10				
		MEM_0A_CKE0,MEM_0A_CKE1,MEM_0B_CKE0,MEM_0B_CKE1					
		pull 90.0ohm to GND(R936,R937,R938,R939)					



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